AMIGA AUCKLAND INC.
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ROYAL OAK 1030
AUCKLAND, NEW ZEALAND

A500 SERVICE TRAINING

AMIGA AUCKLAND INC.
PO
ROYA
AUCKLAND, NEW ZEALAND

Venue Commodore Business Machines
Unit 13/1, 663 Victoria Street
Abbotsford, VIC 3067

Date 19 SEP 1989

Lecturer Randy Chow M.Eng.Sc. B.A.Sc MIEEE
(Technical Support Manager)

COURSE OUTLINE

This training course is designed to help service technicians better understand the hardware and component level repair of the A500 Computer.It assumes a basic computer and electronic knowledge as well as the basic operation of the computer.

A500 Technical specifications

Power supply specifications

68000 Microprocessor

- Basic Architecture
- Interface signals
- Data organization in memory

Custom Chips, Features and functional block diagrams

- Paula
- Denise
- Fat Agnus
- Gary

Theory of operations

- System clock sub-system
- ROM sub-system
- Keyboard
- Keyboard interface

Theory of operations cont'

- Mouse interface
- Display interface
- Floppy disk drive
- Floppy drive interface
- Audio sub-system
- Printer interface
- RS232 interface
- Real Time Clock interface
- RAM sub-system
- Expansion RAM sub-system

System Block Diagram

RAM Access

- 68000 chip Ram access
- Agnus chip Ram access

System Memory Map

Common troubleshooting approaches

- Software
- Hardware
- Others

Common Faults

Power up self-test

- Power up self-test
- Keyboard power up self-test

Diagnostics

- System Diagnostic
- Rom based diagnostic

Waveform Comparison

DRAM Refresh waveform

Chip/Expansion Ram swaps

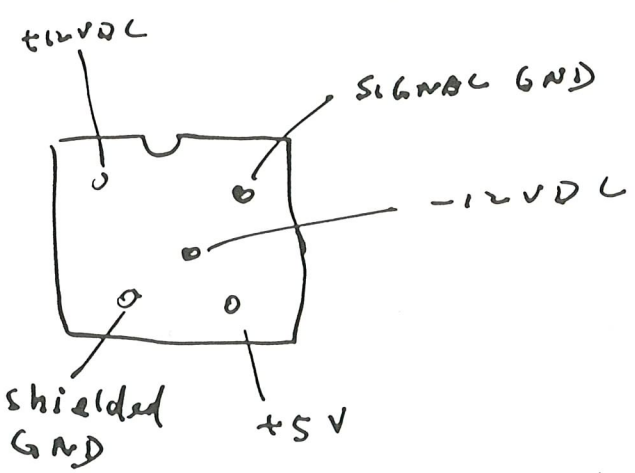
NO-OPT 68000

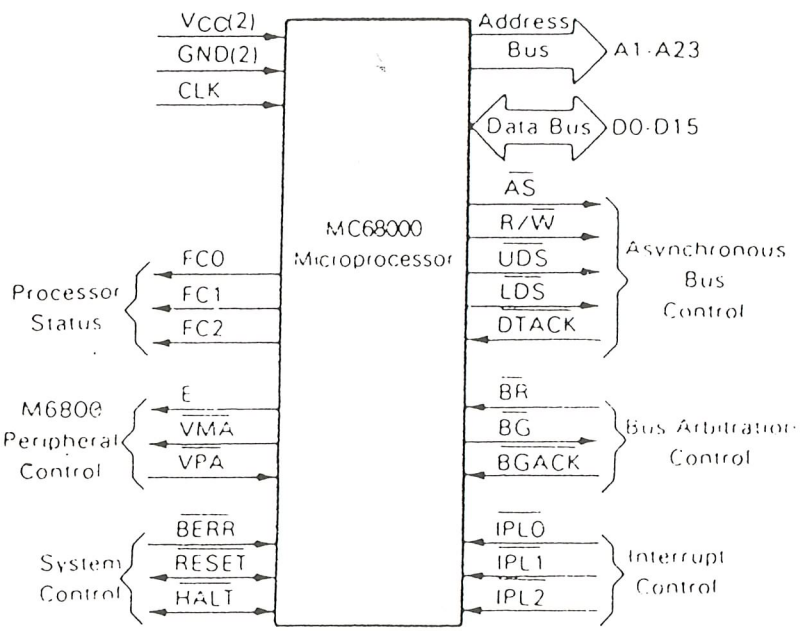
Disk drive alignment

A500 POWER SUPPLY SPECIFICATIONS

AC INPUT	216 - 264 VAC	
AC FREQ	47 - 53 Hz	
DC OUTPUT	5 V	4.5 A MAX
	12 V	1.0 A MAX
	-12 V	0.1 A MAX
MAX POWER	35 WATTS	

CONNECTOR PIN OUT




VCC(2)
GND(2)
CLK
MC68000
Microprocessor
Address
Bus
A1-A23
Data Bus
D0-D15
AS
R/W
UDS
LDS
DTACK
Asynchronous
Bus
Control
Processor
Status
FC0
FC1
FC2
M6800
Peripheral
Control
E
VMA
VPA
BR
BG
BGACK
Bus Arbitration
Control
System
Control
BERR
RESET
HALT
IPL0
IPL1
IPL2
Interrupt
Control

68000 SIGNAL DESCRIPTION

A1 – A23 : ADDRESS BUS
23 BIT ADDRESS 16M BYTE
DURING INTERRUPT A1 – A3 INDICATE LEVEL OF INT

DO – D15 : 16 BIT DATA BUS, TRANSFER DATA IN BYTE OR WORD

AS ADDRESS STROBE : VALID ADDRESS ON ADDRESS BUS

UDS UPPER DATA STROBE
LDS LOWER DATA STROBE

UDS	LDS	D8 – D15	DO – D7
0	1	VALID	NOT VALID
1	0	NOT VALID	VALID
0	0	VALID	VALID

D TACK DATA TRANSFER ACKNOWLEDGE
DEVICE → CPU

BR	BUS REQUEST	DEVICE → CPU
BG	BUS GRANT	CPU → DEVICE
B GACK	BUS GRANT ACK.	DEVICE → CPU

IPLO, IPL1, IPL2 INTERRUPT CONTROL
7 LEVEL OF INTERRUPT

BERR BUS ERROR DEVICE → CPU

RESET RESET, BI – DIRECTIONAL
TOTAL SYSTEM RESET REQUIRES HALT & RESET

HALT DEVICE → CPU, BUSES & CONTROL ⇒ TRI STATE

DATA REGISTERS DO – D7
CAN BE USED FOR BYTE, WORD, LONG WORD DATA OPERATIONS

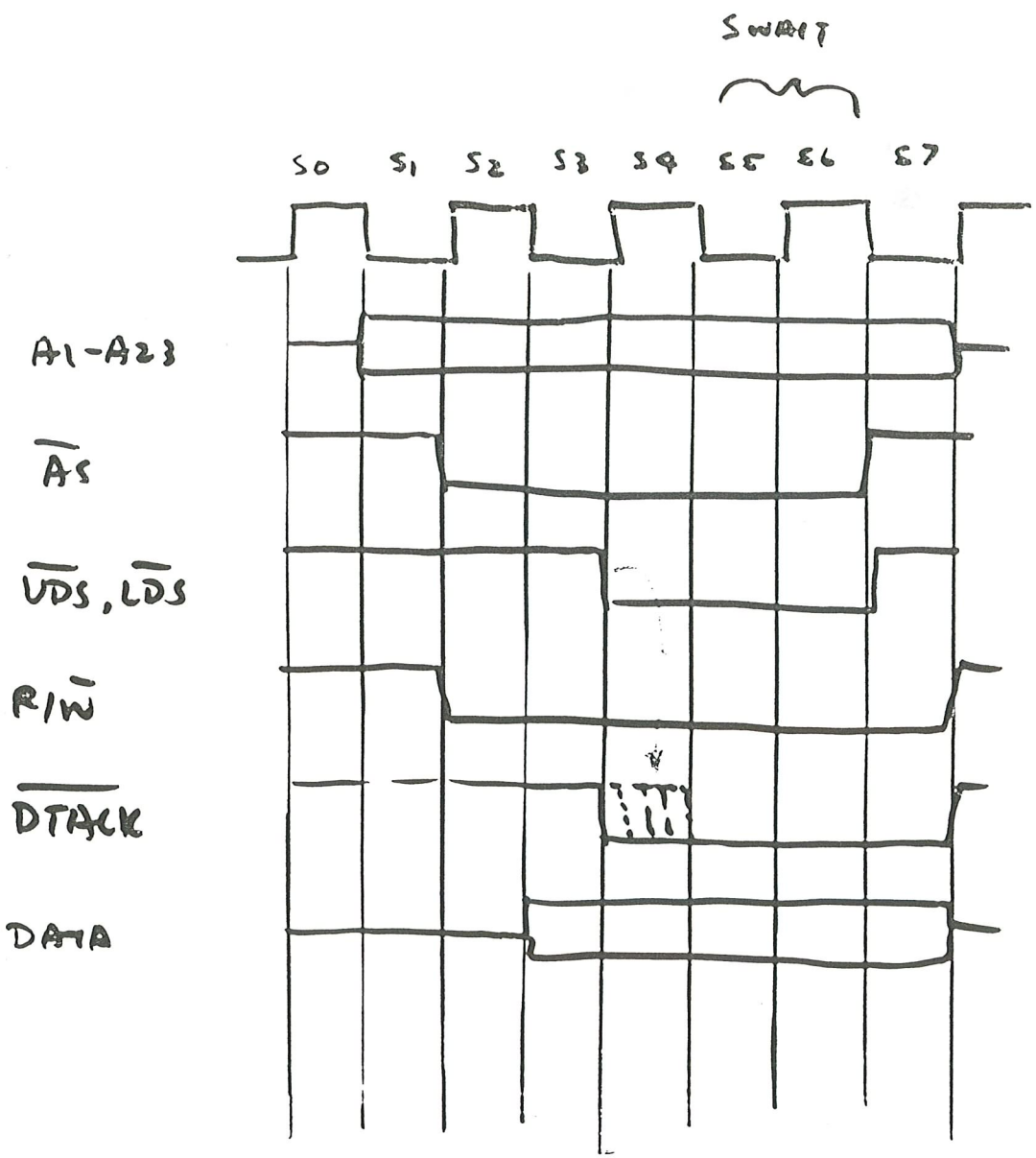
ADDRESS REGISTERS A0 – A7

USED FOR:

- BASE ADDRESS REGISTERS
- WORD ADDRESS
- LONG WORD ADDRESS
- INDEX REGISTER

STACK POINTER A7

{ A7 USER STACK POINTER
{ A7′ SUPERVISOR STACK POINTER



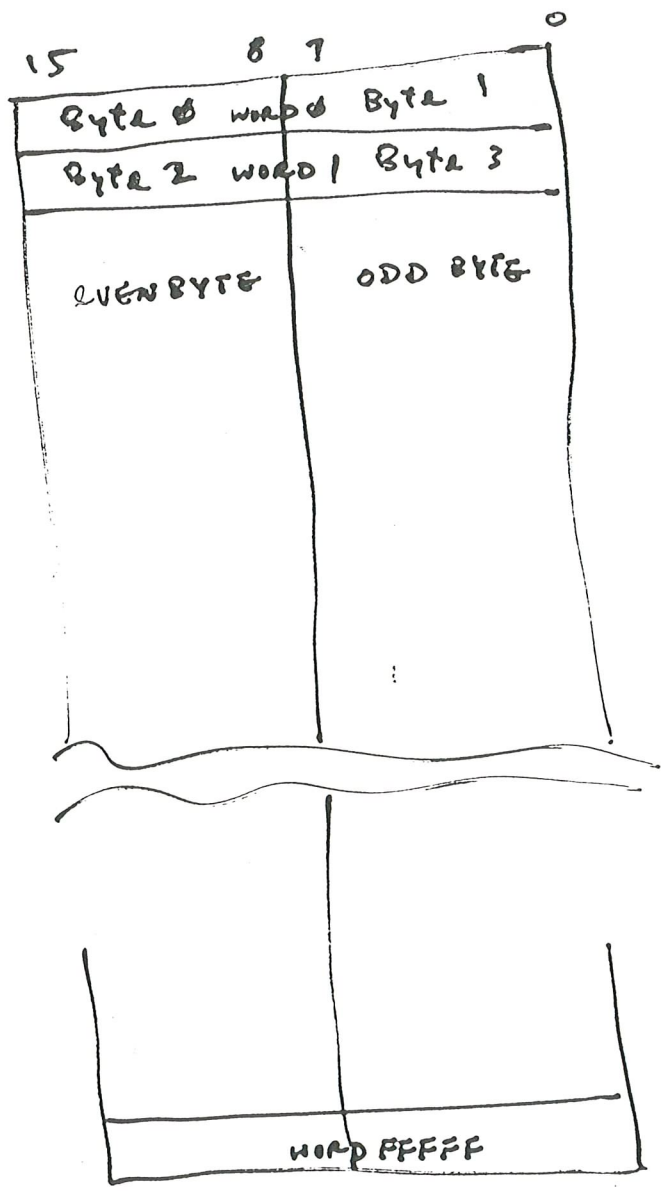
7MHz ⇒

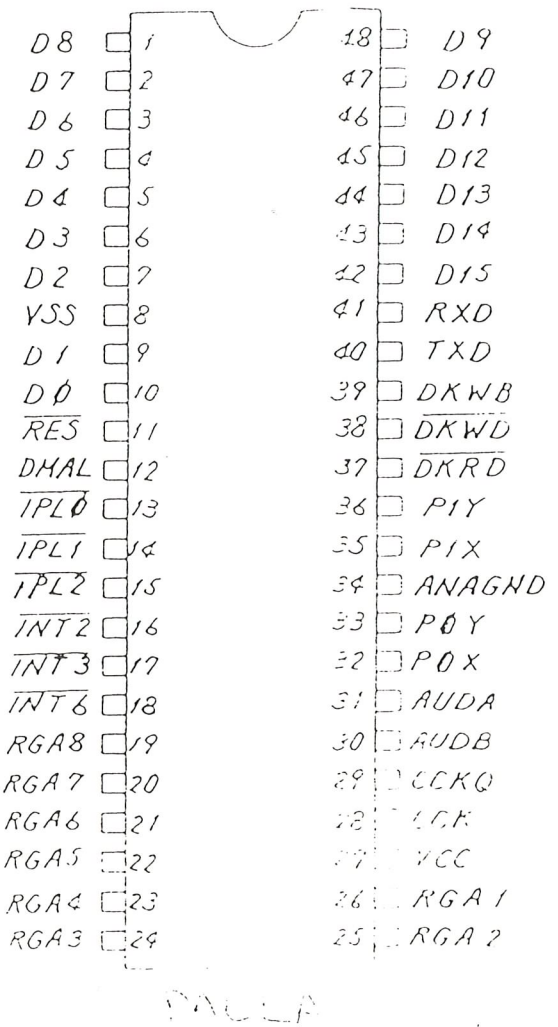
S0+S1 = 280ns

8 x 140 = 1120 ns

68000 WRITE TIMING

DATA ORGANIZATION IN MEMORY
FOR 68000 SYSTEM




D8 1
D7 2
D6 3
D5 4
D4 5
D3 6
D2 7
VSS 8
D1 9
D0 10
RES 11
DHAL 12
IPL0 13
IPL1 14
IPL2 15
INT2 16
INT3 17
INT6 18
RGA8 19
RGA7 20
RGA6 21
RGA5 22
RGA4 23
RGA3 24
48 D9
47 D10
46 D11
45 D12
44 D13
43 D14
42 D15
41 RXD
40 TXD
39 DKWB
38 DKWD
37 DKRD
36 P1Y
35 P1X
34 ANAGND
33 P0Y
32 P0X
31 AUDA
30 AUDB
29 CCKQ
28 CCK
27 VCC
26 RGA1
25 RGA2

PAULA 8364

PORTS, AUDIO, UART, CHIP

37 REGISTERS

MAIN FEATURES

4 AUDIO CHANNELS. GENERATE COMPLEX
AM OR FM WAVEFORM

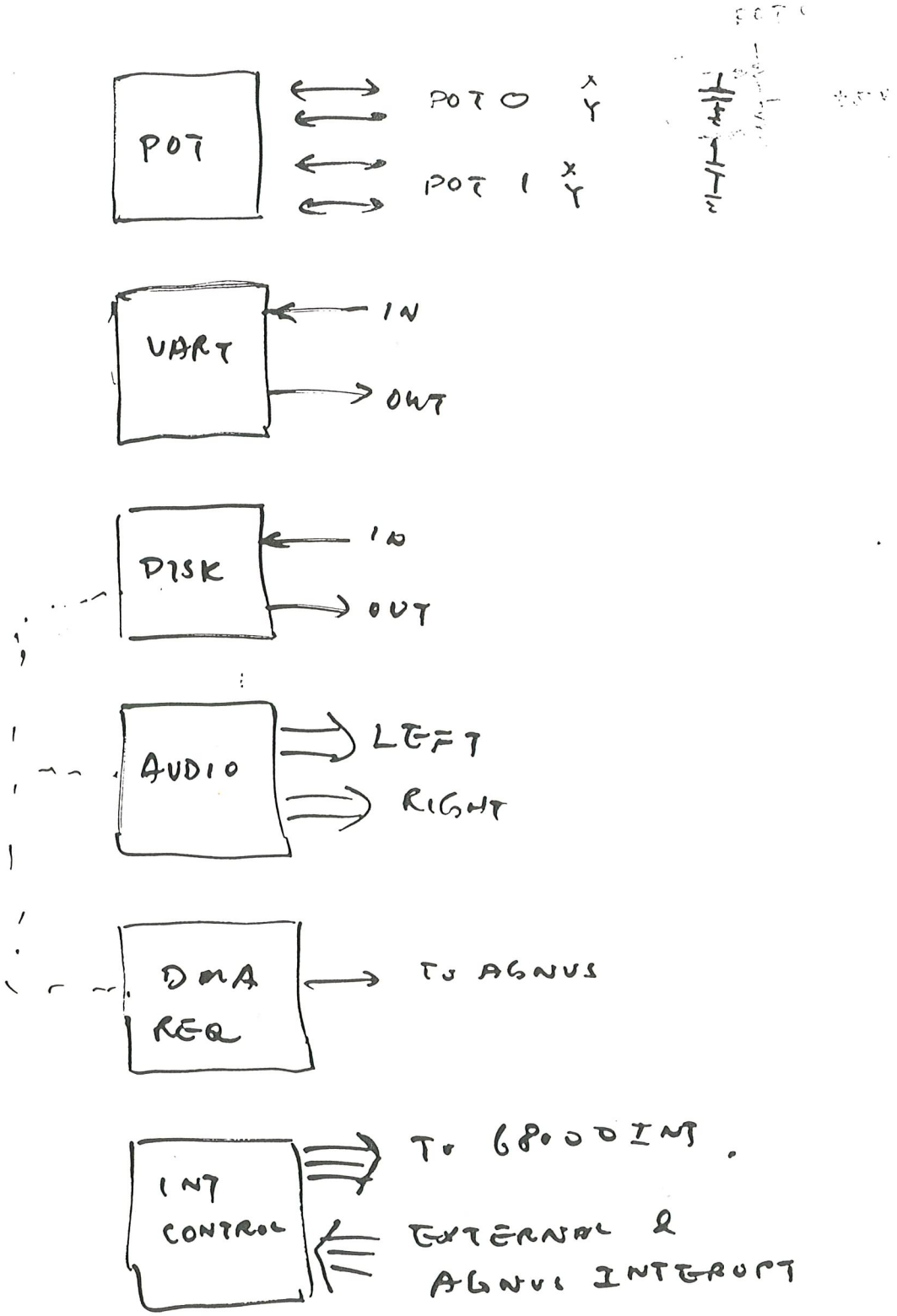
SERIAL PORT UART

DISK I/O PORT

POT I/O PORT (PROPORTIONAL CONTROLLER)

INTERRUPT CONTROL, 6 LEVEL

PAULA BLOCK DIAGRAM



AUDIO BLOCK – 4 CHANNELS
– EACH CHANNEL HAS ITS DMA, DATA, FREQ, VOL REGISTERS
– D TO A CONVERTER

DISK BLOCK – 3 REGISTERS: READ, WRITE, CONTROL

– DATA PRE COMPENSATION FOR O/P

– DATA SEP AND PLLFOR I/P

SERIAL BLOCK – REGs, DATA
CONTROL
TRANSMIT
RECEIVE

POT BLOCK – COUNTER CONVER TIME TO DATA CAP CHARGING

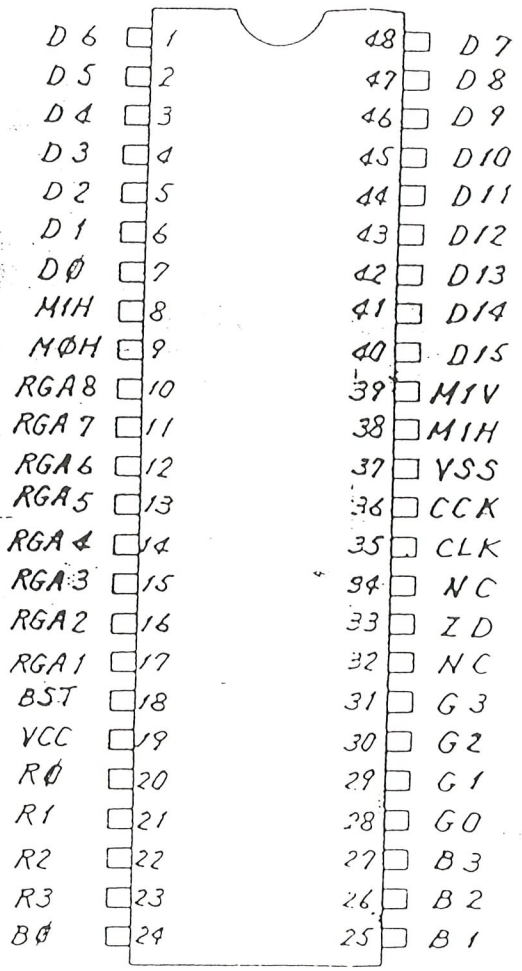
AUDIO AND DISK CONTROLLER USES DMA

DENISE 8362

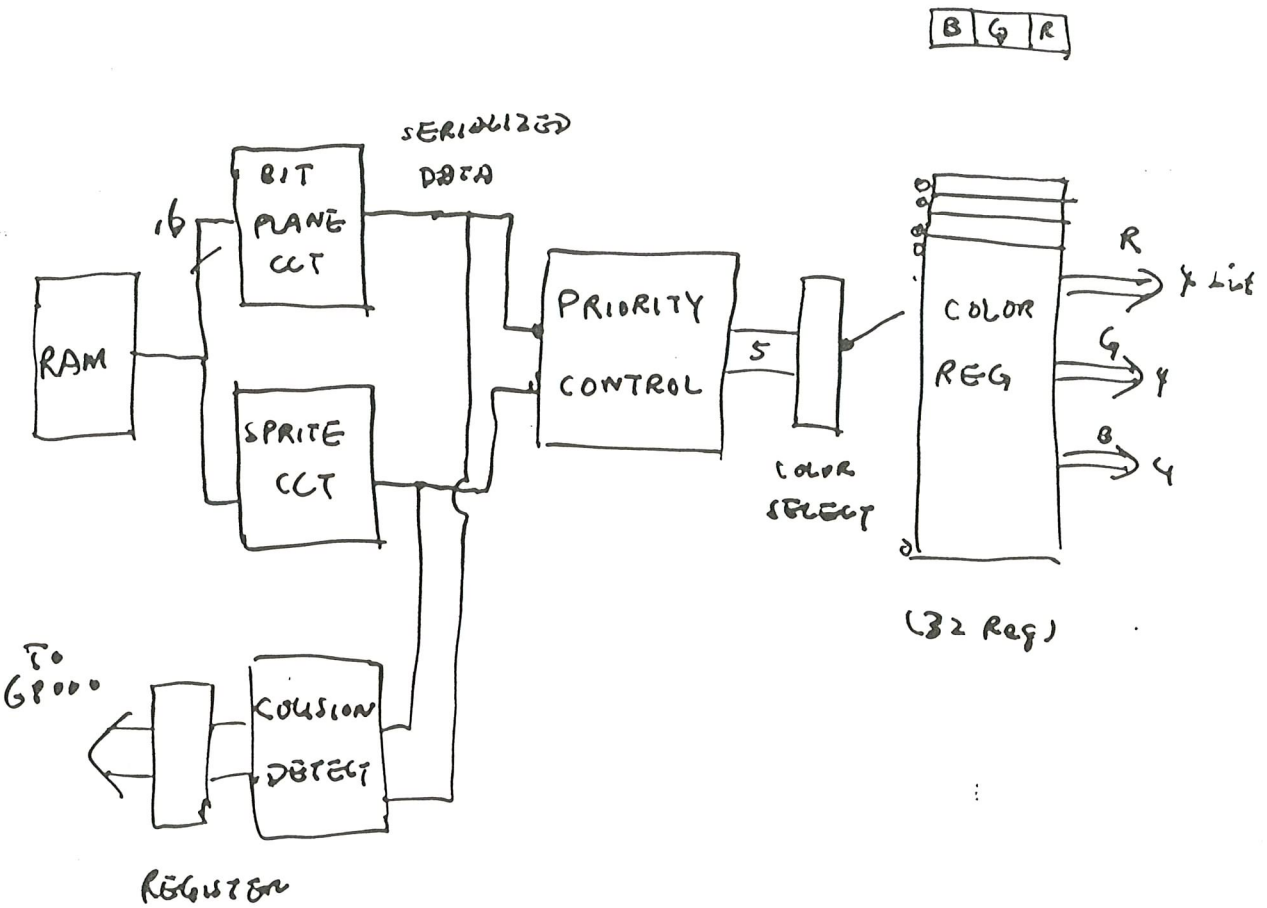
DISPLAY ENCODER

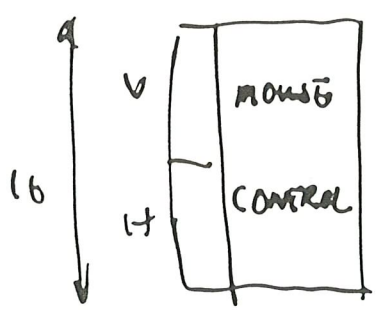
- 83 REGISTERS
- MAIN FEATURES
- SELECT OBJECT FOR DISPLAY
- ENCODE OBJECT TO RED, BLUE AND GREEN COLOR CODE
- RESOLUTION 320 X 200 TO 640 X 400
  4096 COLORS
  SPRITE CONTROLLER

- DISPLAY BOTH BIT PLANE IMAGE AND SPRITE
- MOUSE INTERFACE


D6 1
D5 2
D4 3
D3 4
D2 5
D1 6
DØ 7
M1H 8
MØH 9
RGA8 10
RGA7 11
RGA6 12
RGA5 13
RGA4 14
RGA3 15
RGA2 16
RGA1 17
BST 18
VCC 19
RØ 20
R1 21
R2 22
R3 23
BØ 24
48 D7
47 D8
46 D9
45 D10
44 D11
43 D12
42 D13
41 D14
40 D15
39 M1V
38 M1H
37 VSS
36 CCK
35 CLK
34 NC
33 ZD
32 NC
31 G3
30 G2
29 G1
28 GO
27 B3
26 B2
25 B1

DENISE

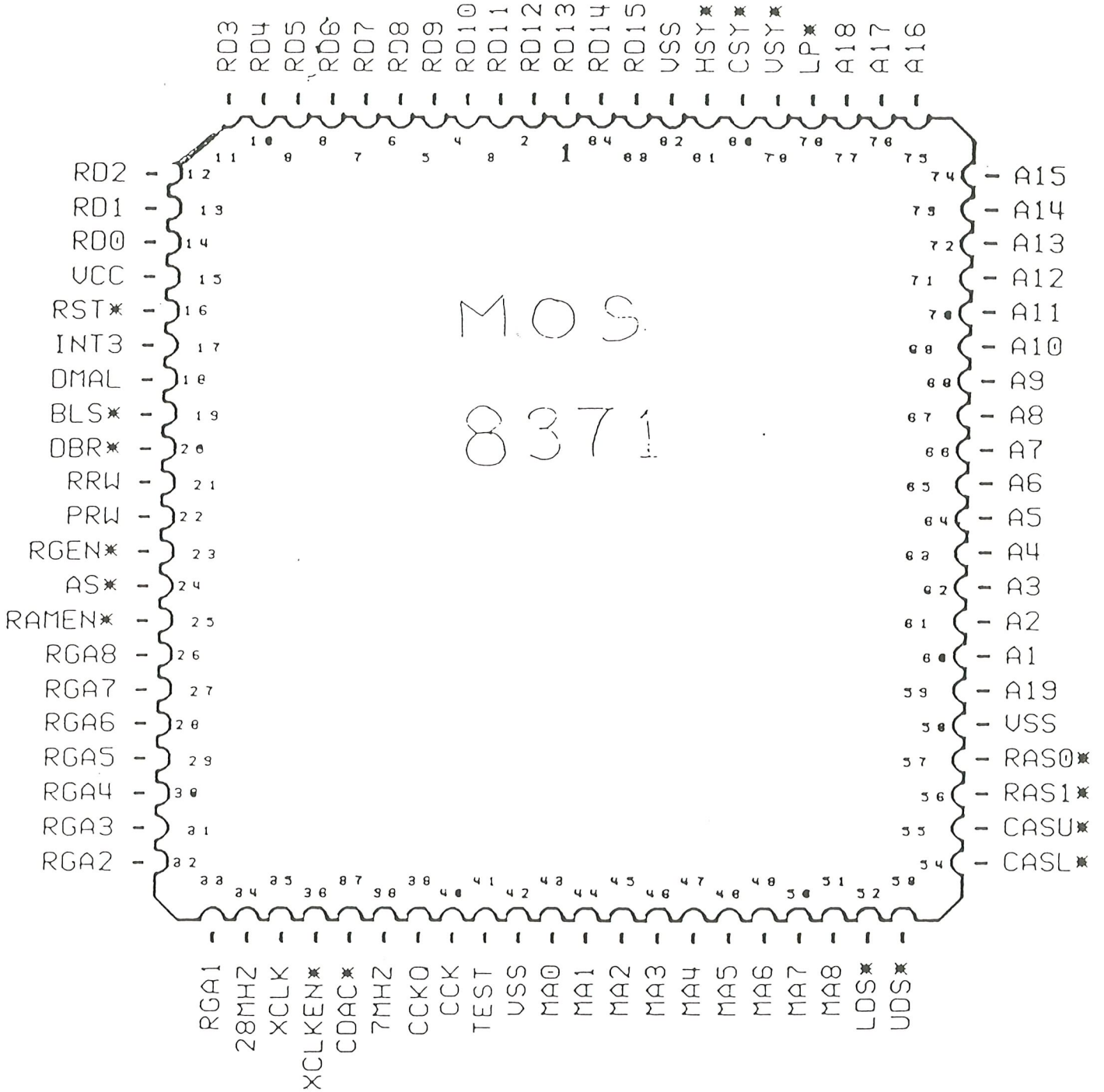




DENISE BLOCK DIAGRAM

Custom Animation Chip

Fat Agnus



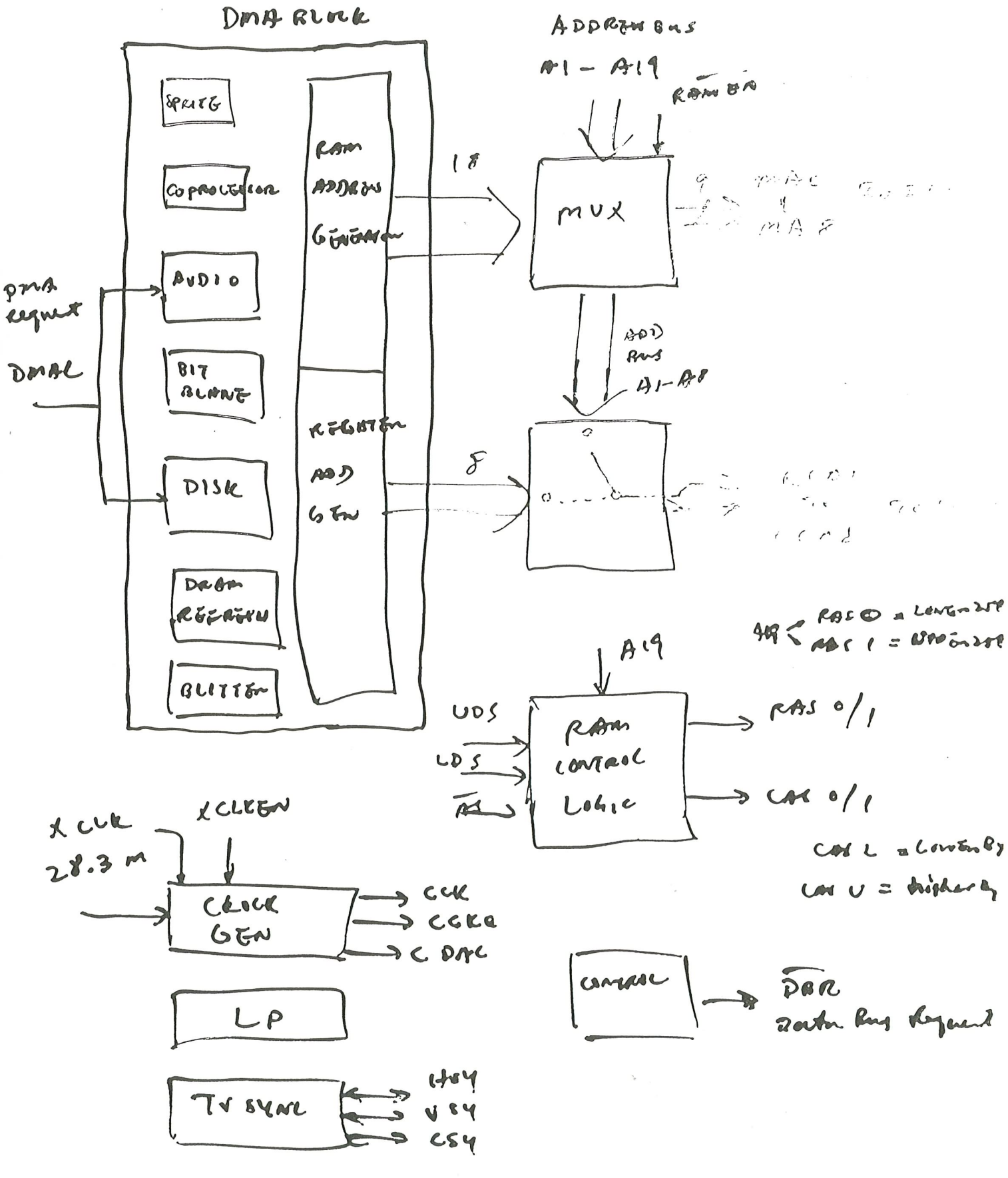
FAT AGNUS

ADDRESSS GENERATOR CHIP

MAIN FEATURES

- BITBLITTER ; MOVE DISPLAY DATA TO ALLOW HIGH SPEED ANIMATION
- CO - PROCESSOR ; CAN CONTROL 3 CUSTOM CHIPS DIRECTLY W.R.T. VIDEO BEAM
- CONTROL 25 DMA CHANNELS
- CLOCK CIRCUITRY
- RAM CONTROL SIGNALS (BOTH VIDEO AND EXP.)
- DRAM MULTIPLEXING ( )
- 103 REGISTERS

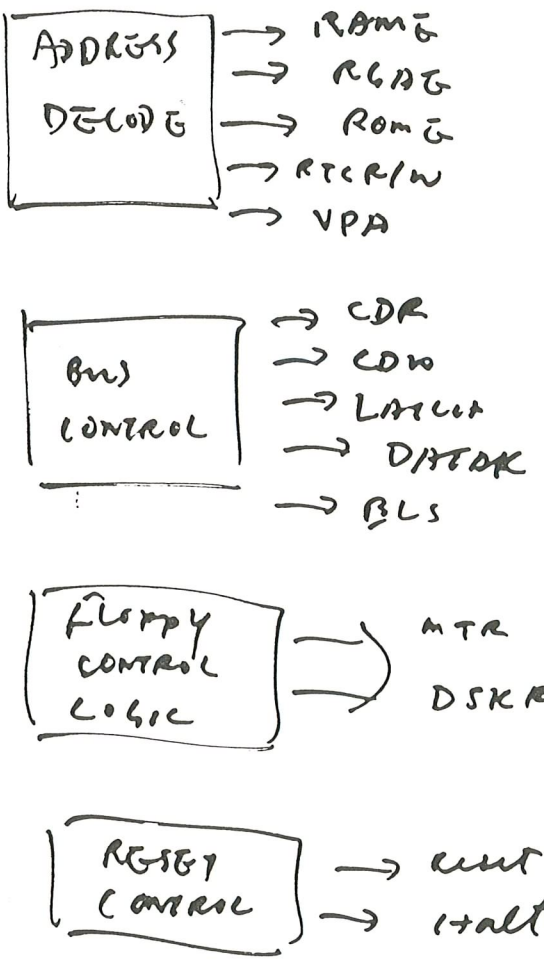
AGNUS BLOCK DIAGRAM



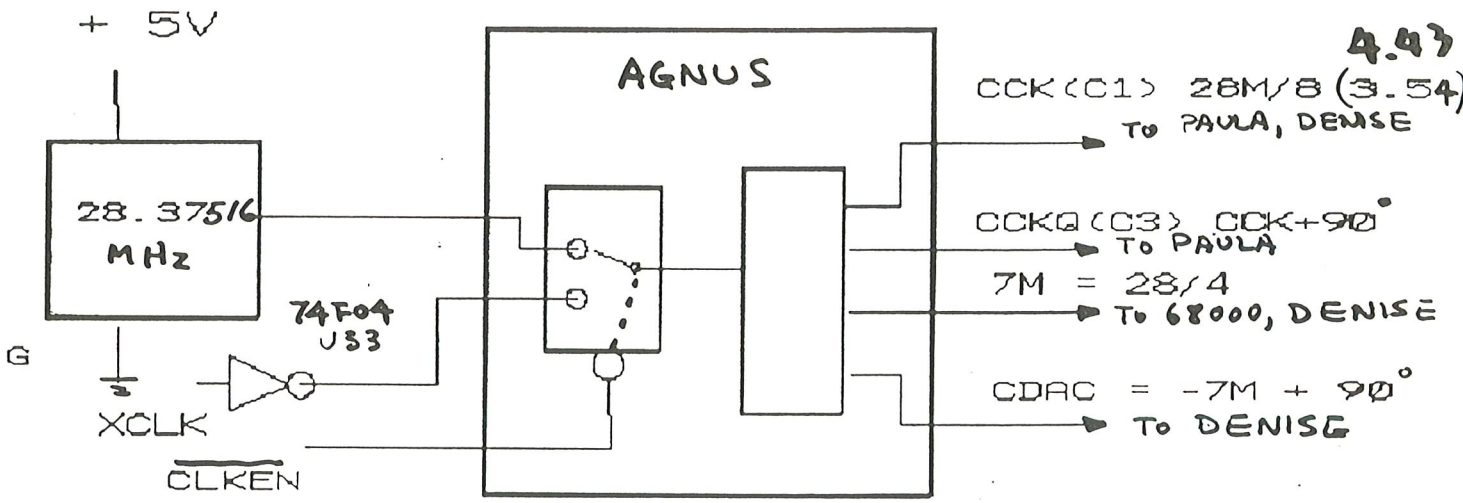
GARY

MAIN FEATURES

- PROVIDE ALL BUS CONTROL SIGNAL
- PROVIDE ALL ADDRESS DECODING
- HANDLES SOME FLOPPY CIRCUIT
- KEYBOARD RESET INTERFACE

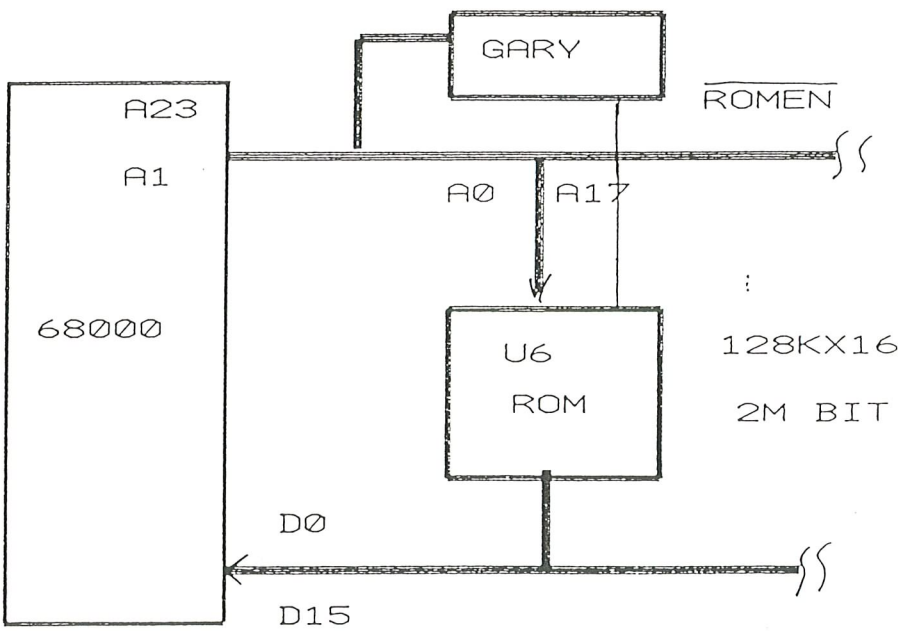


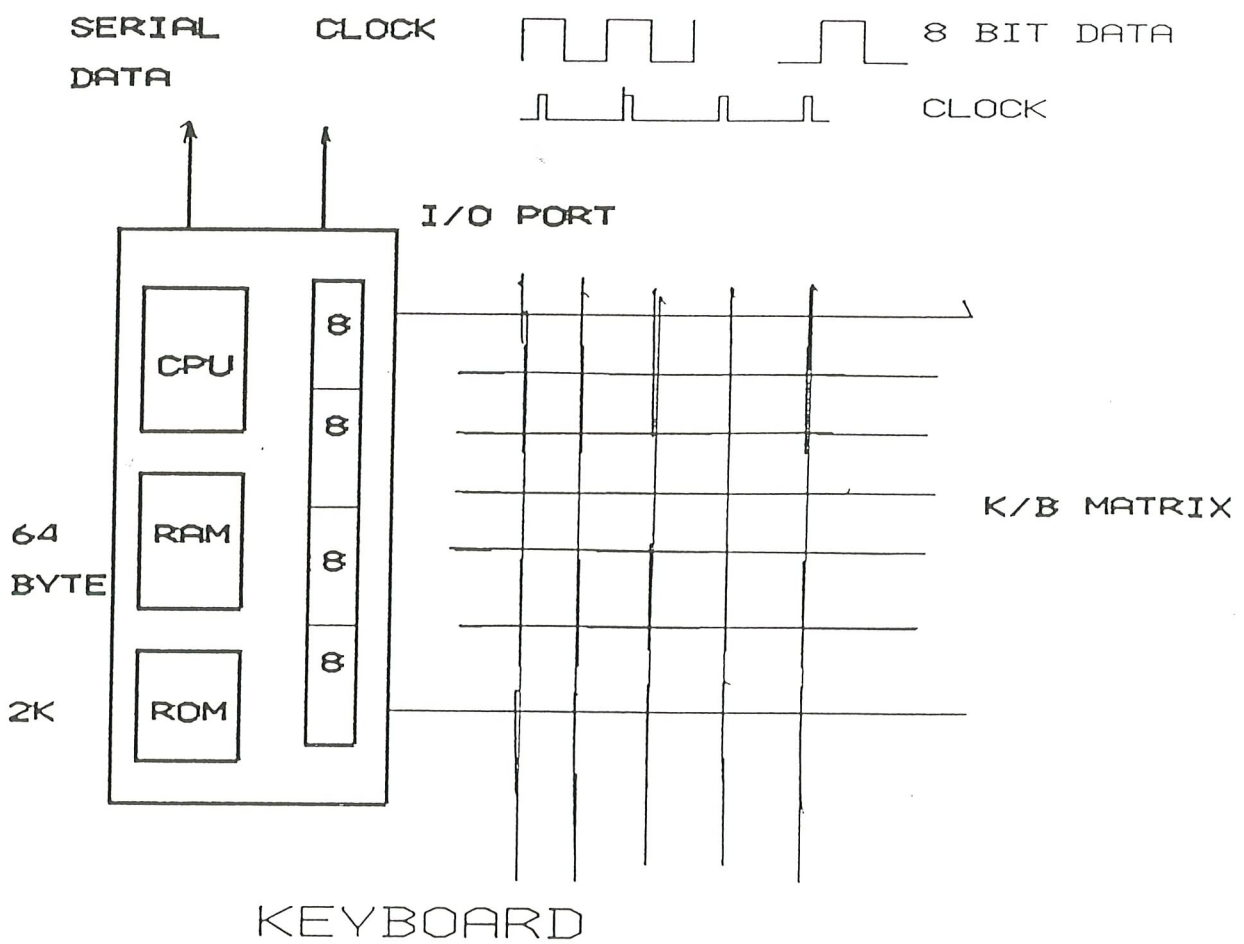
CLOCK CIRCUITRY



4.43

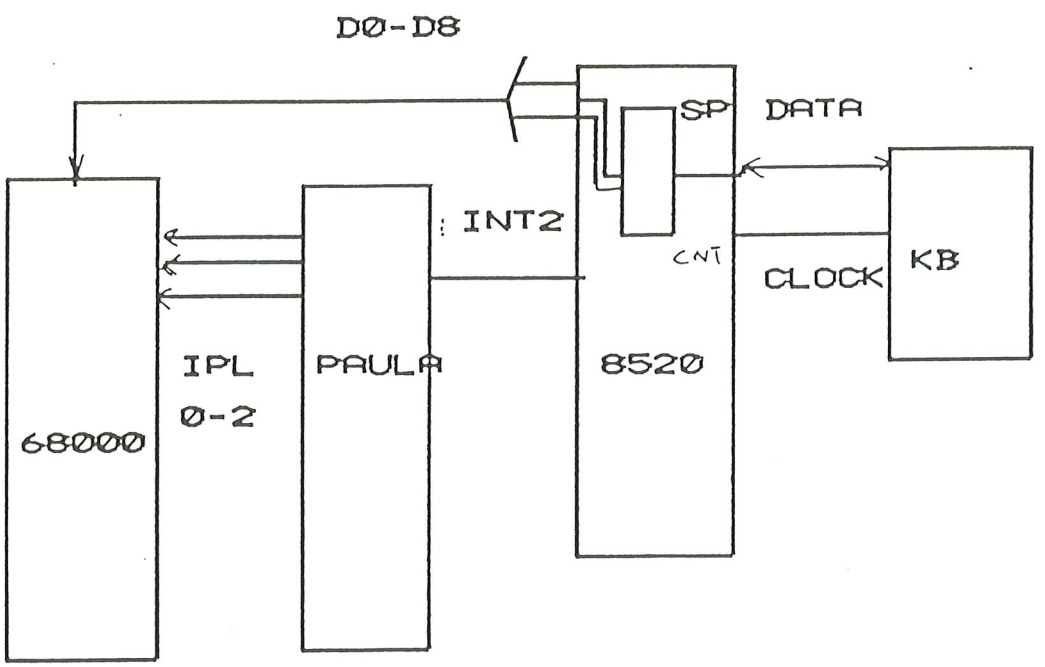
ROM SUB-SYSTEM



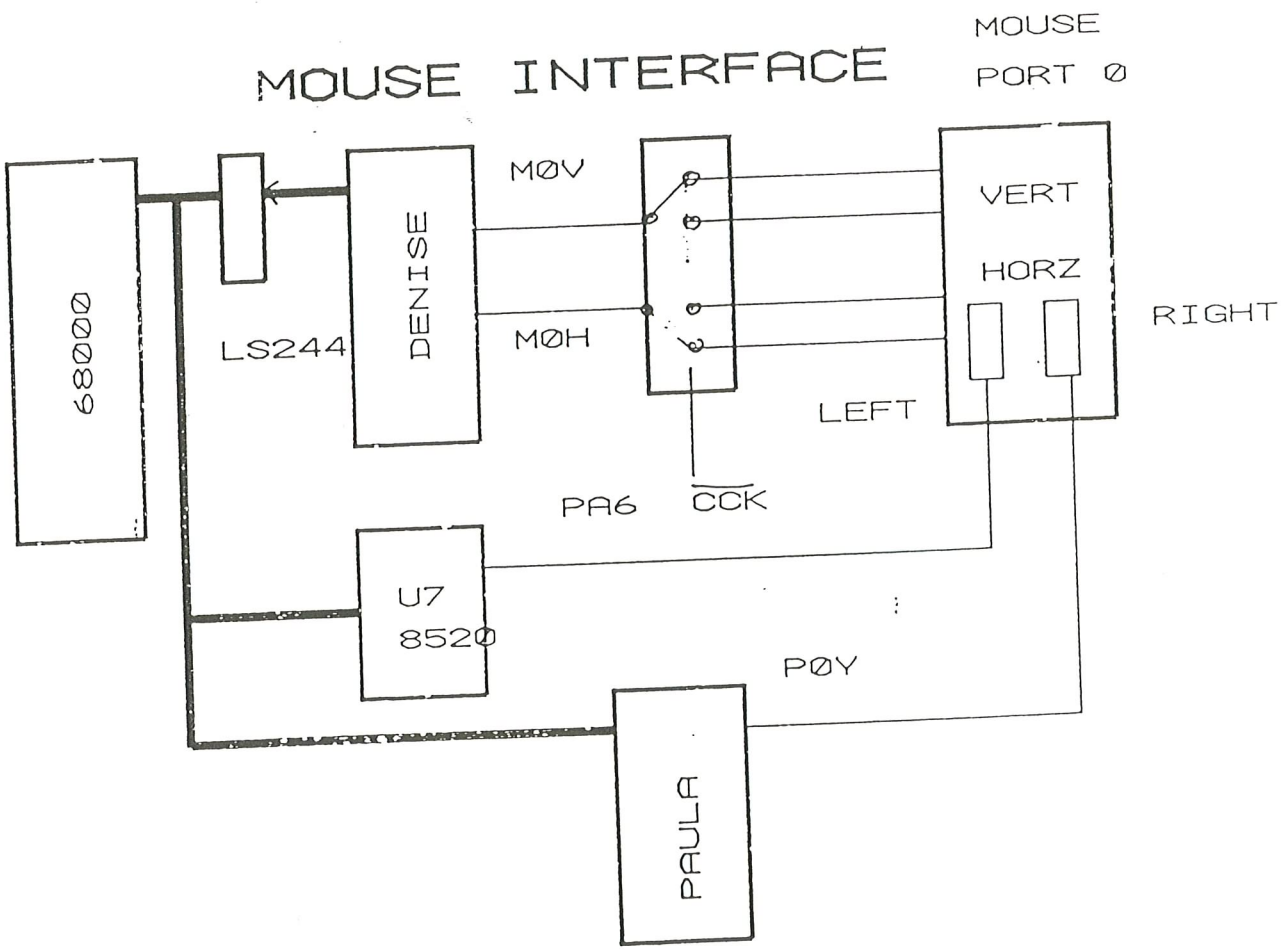

SERIAL DATA
CLOCK
8 BIT DATA
CLOCK
I/O PORT
CPU
RAM
ROM
64 BYTE
2K
8
8
8
8
K/B MATRIX

KEYBOARD

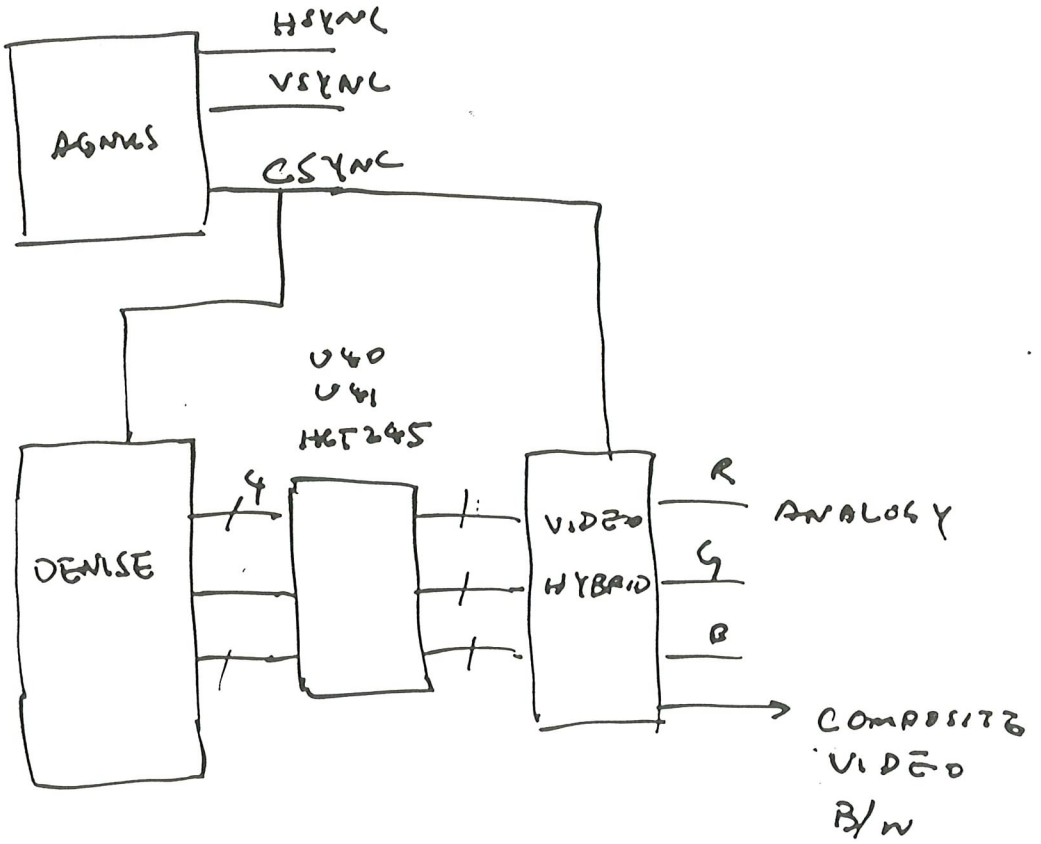
KEYBOARDD INTERFACE



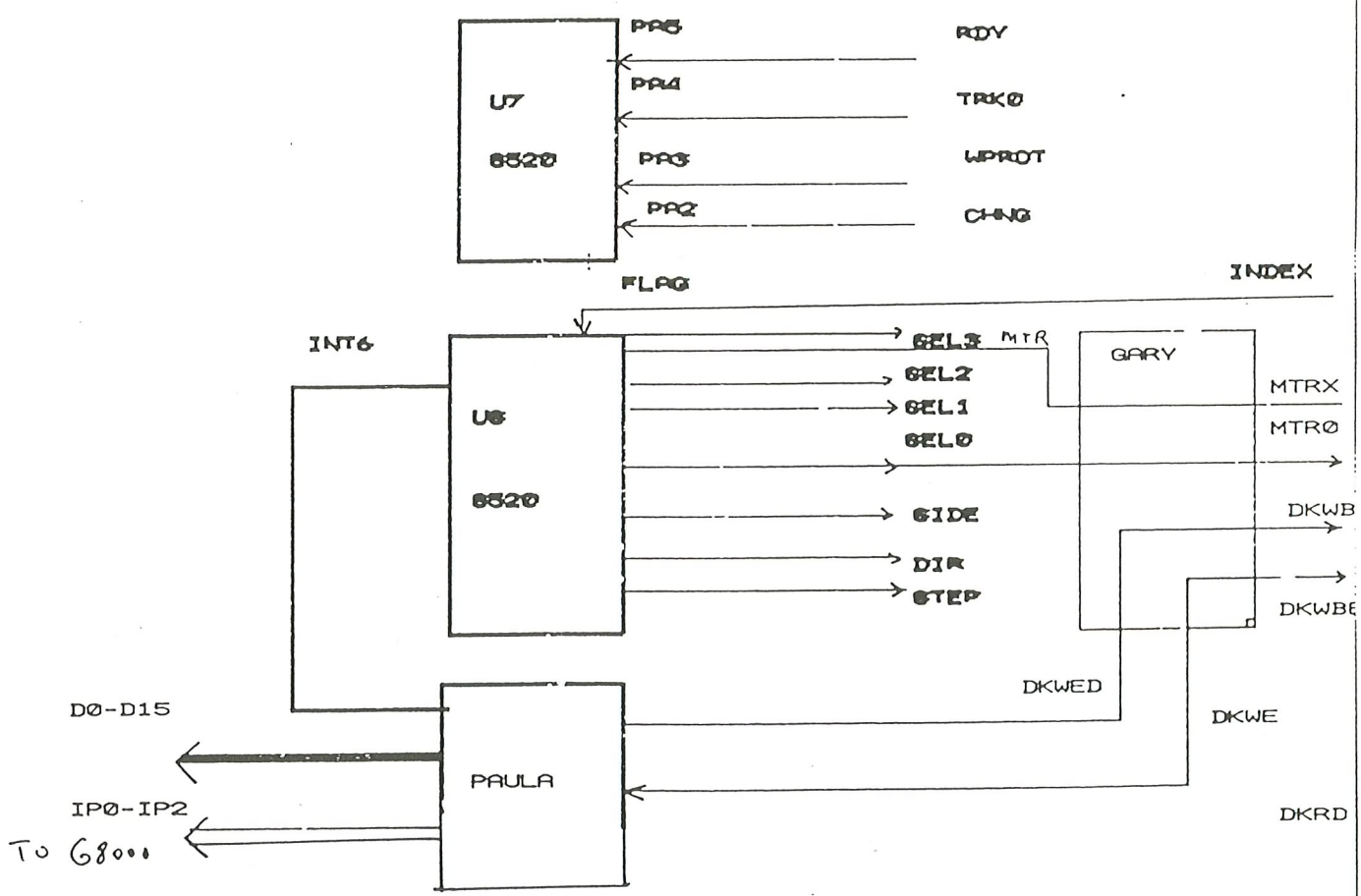
MOUSE INTERFACE



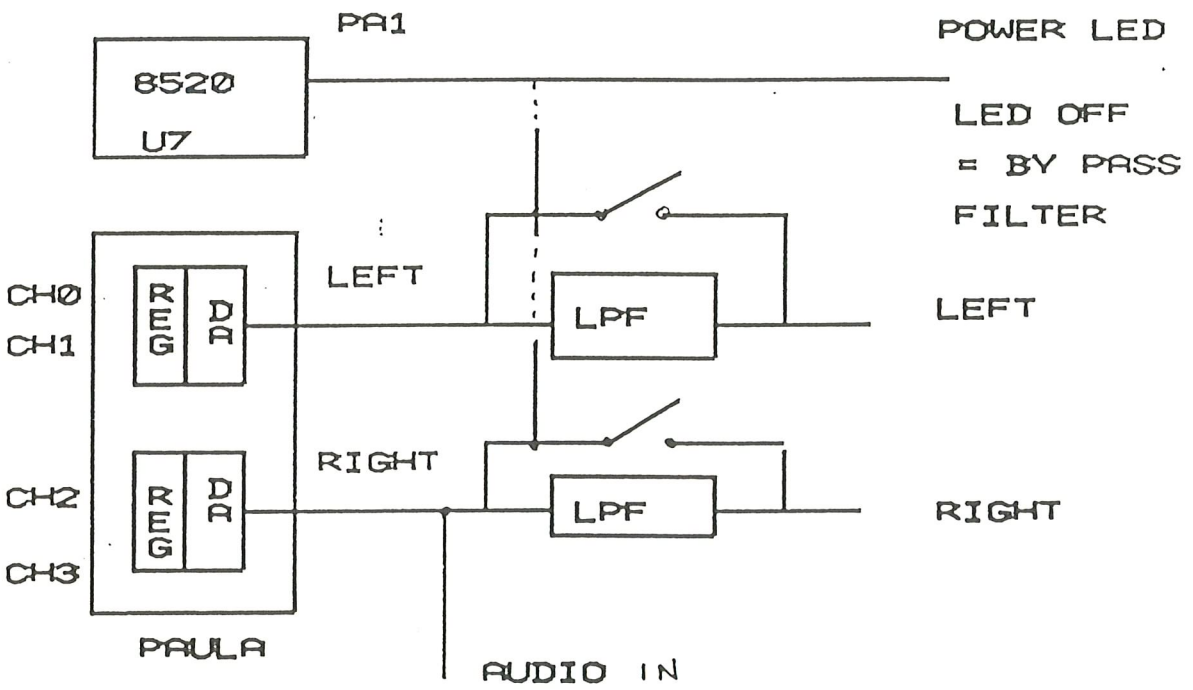
VIDEO INTERFACE



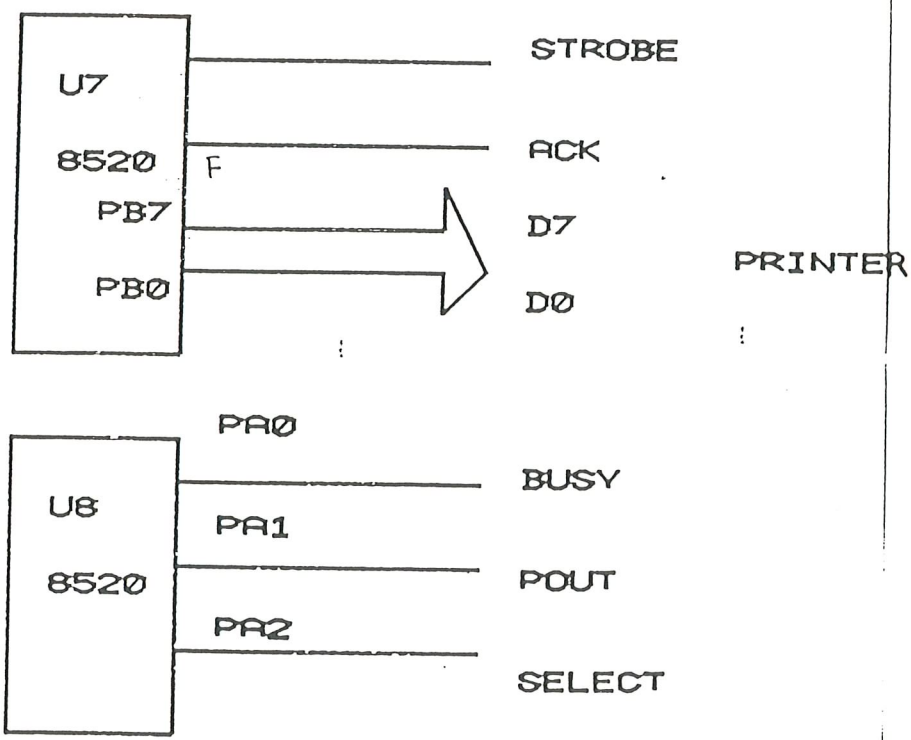
FLOPPY DRIVE INTERFACE



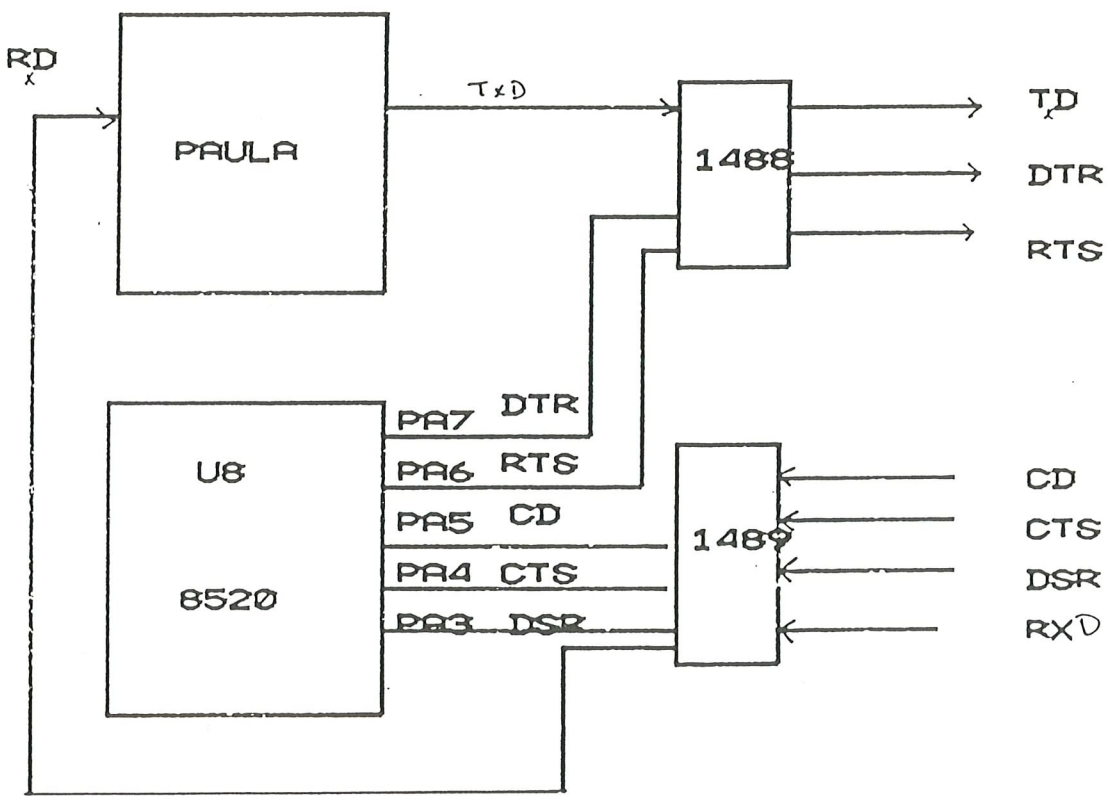
AUDIO SUB-SYSTEM



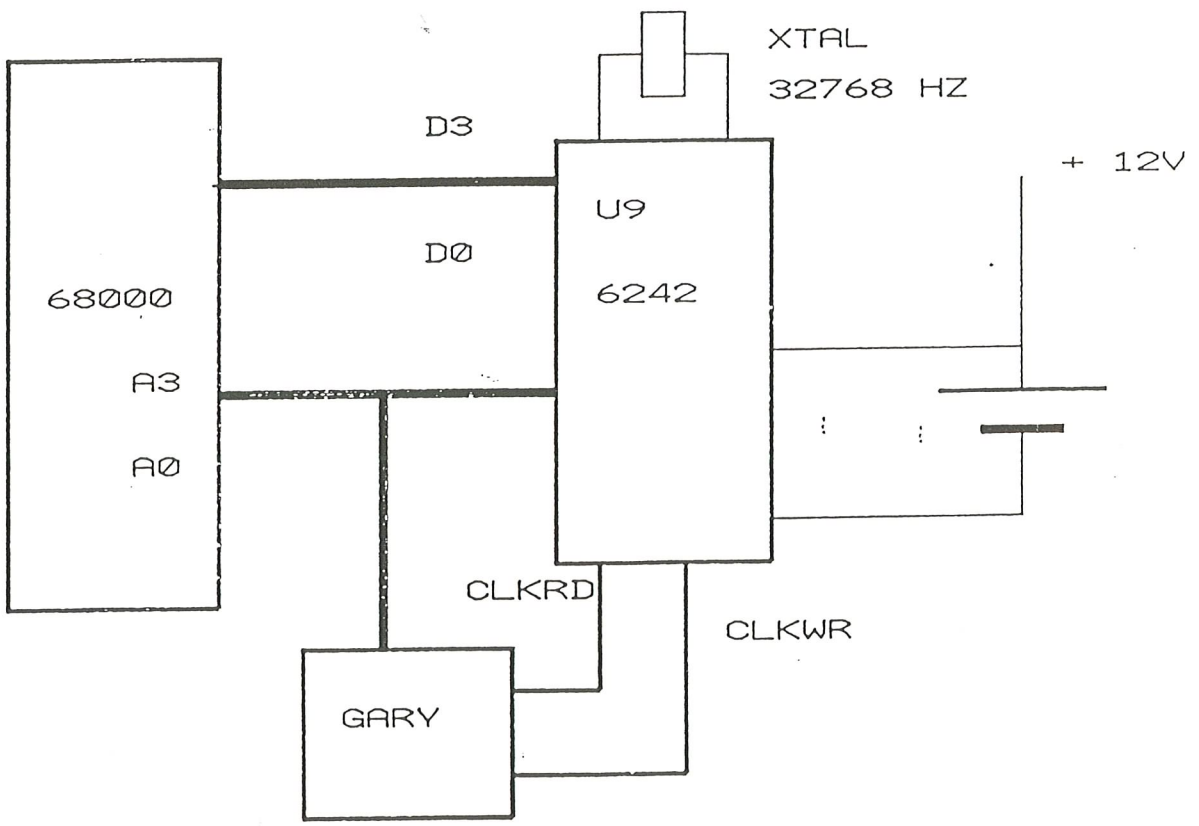
PRINTER INTERFACE

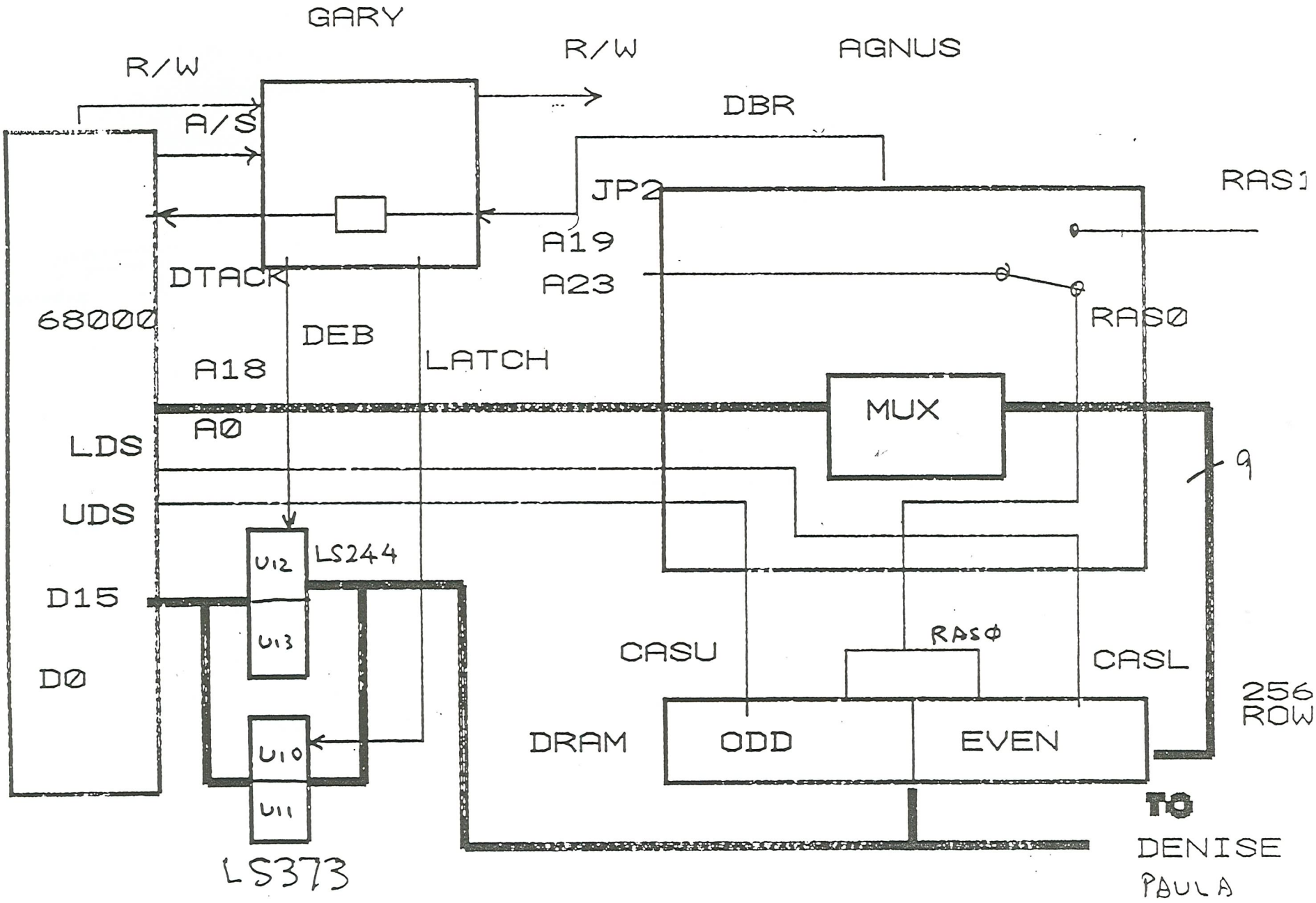


RS232 INTERFACE

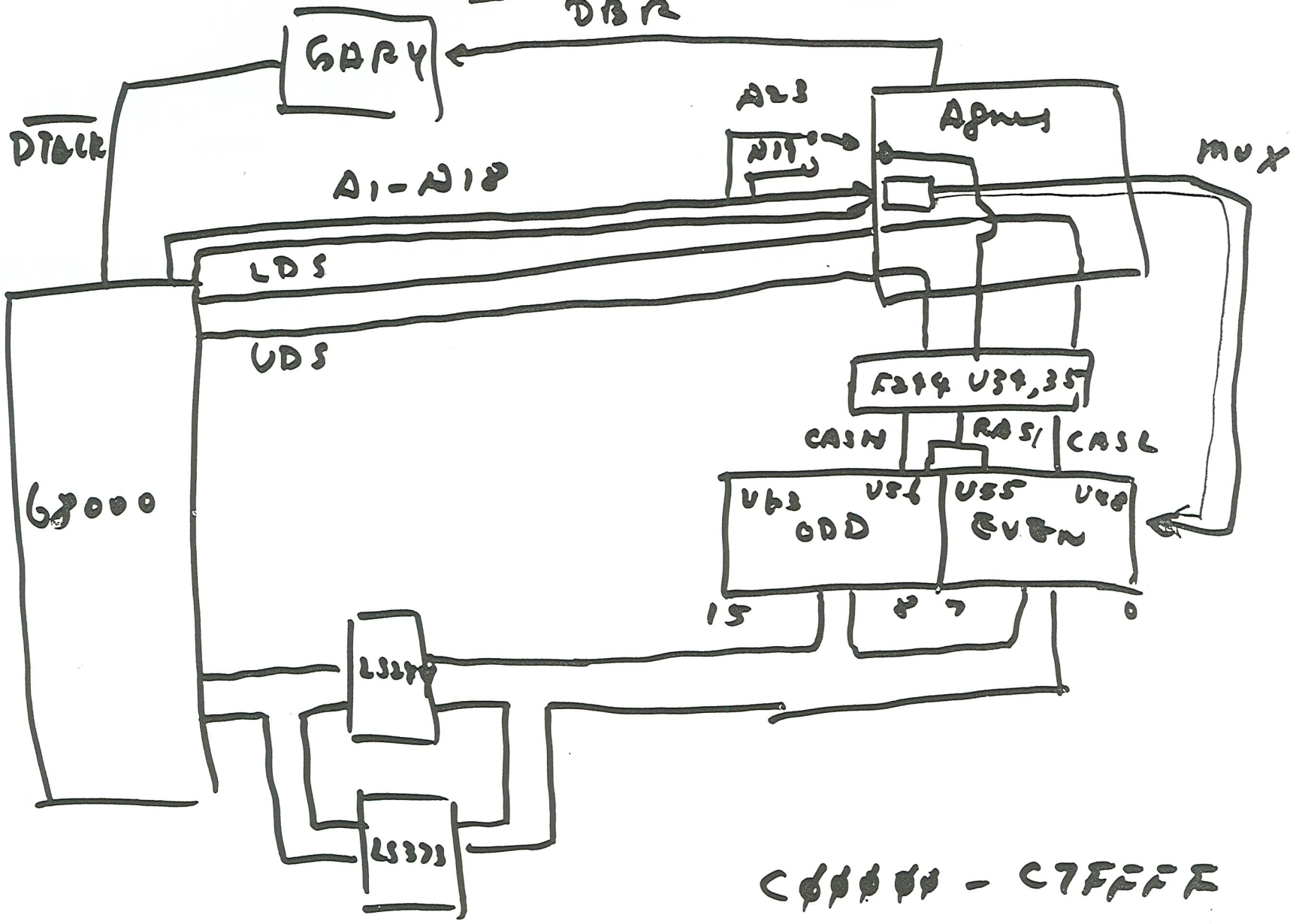


REAL TIME CLOCK




GARY
R/W
R/W
AGNUS
A/S
DBR
JP2
RAS1
A19
A23
DTACK
RAS0
68000
DEB
LATCH
A18
MUX
A0
LDS
9
UDS
U12
LS244
D15
U13
RASΦ
CASU
CASL
D0
256
ROW
U10
DRAM
ODD
EVEN
U11
TO
DENISE
PAULA
LS373

EXPANSION RAM

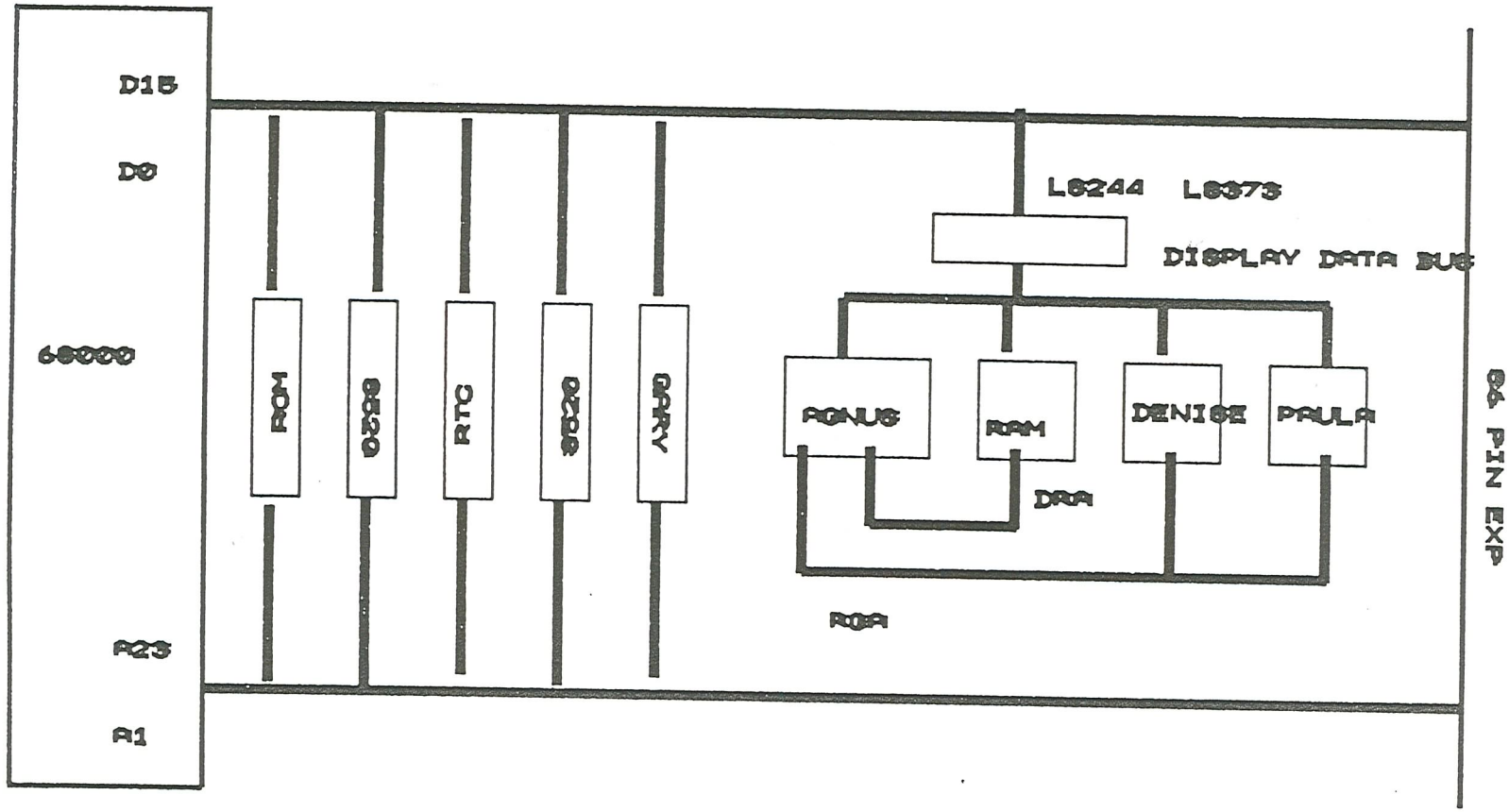


C00000 - C7FFFF

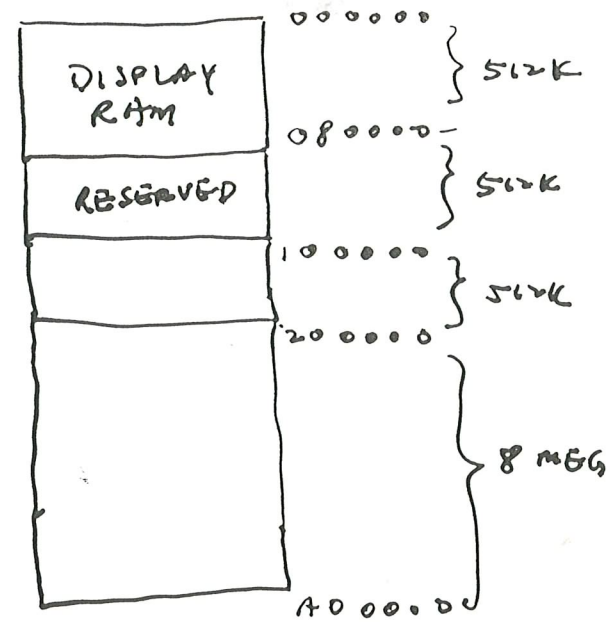
512 KByte

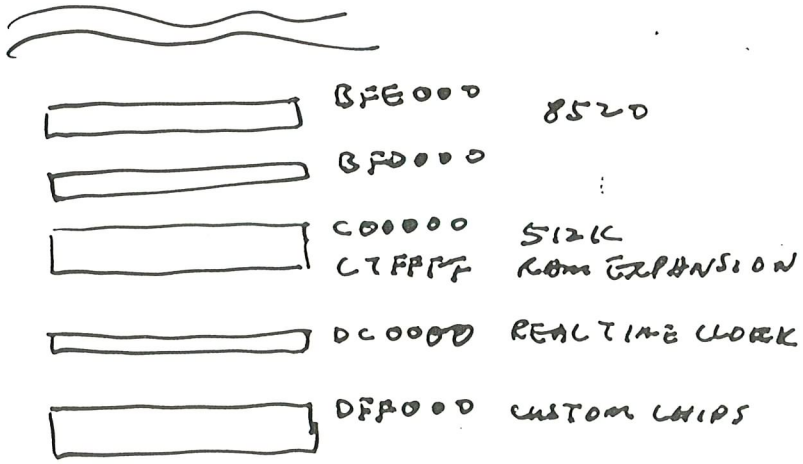
256 K word

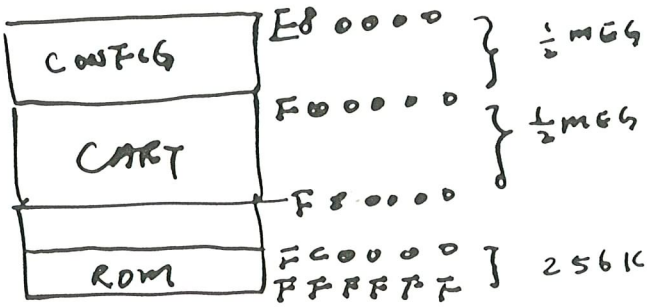
A500 SYSTEM BLOCK DIAGRAM



A500 MEMORY MAP







SOFTWARE APPROACH

- POWER UP DIAGNOSTIC
- ROM BASED DIAGNOSTIC
- DISK BASED DIAGNOSTIC

HARDWARE APPROACH

- REQUIRE TROUBLESHOOTING TOOLS
- DMM DIGITAL MULTIMETER
- LOGIC PROBE (GOOD FOR LOW FREQUENCY PULSES)
- OSCILLOSCOPE
- LOGIC PULSER – GENERATE PULSES OF OPP. LOGIC LEVEL
- SIGNATURE ANALYSER (HP)
  16 – OR 24 BIT TEST CODE
  SAMPLE THE DATA AT DIFF. PLACES ON A GOOD CIRC. BOARD
- STEADY STATE WAVE FORM COMPARISON
- IN – CIRCUIT TESTING
- NO – OP ANALYSIS
- IN – CIRCUIT EMULATOR

OTHERS

COMMON SENSES; LOOK, SMELL, FEEL

HEAT AND COOL ; TO DETECT INTERMITTENT FAILURE

PIGGY-BACKING; TO DETECT BROKEN BOND INSIDE A CHIP

REPLACING CHIPS ONE AT A TIME;

EFFICIENT FOR SOCKETED CHIPS

MAKES SENSE FOR INEXPENSIVE TTL

EXPERIENCE - FAULT CHART; VERY EFFECTIVE FOR

COMMON FAULTS

FAULTS	CAUSES
GREEN SCREEN	FAT AGNUS SOCKET MEMORY
NO POWER	POWER SUPPLY
CAN'T WRITE TO DISK	DISK DRIVE
PRINTER WON'T WORK	8520, EMI FILTER
WILL NOT LOAD WORKBENCH	8520, DISK DRIVE
2ND J/STICK PORT WON'T WORK	74LS 153
MOUSE WON'T WORK IN ONE DIR.	MOUSE
YELLOW SCREEN	MEMORY FAULT
NO LED	OSC XTAL
HALFWAY LOADING S/WARE	EXP. RAM CART.
WHITE SCREEN	FAT AGNUS
DISK DRIVE READ/WRITE ERROR	CABLE POOR CONTACT
BLACK SCREEN	XTAL

POWER UP DIAGNOSTICS

SEQ	TEST	SCREEN	POSSIBLE CAUSES
1	1/3 SEC. DELAY		
2	JUMP TO ROM CART IF PRESENT (F00000)		
3	DISABLE AND CLR ALL DMA, INT.		
4	CLEAR SCREEN	BLACK	
5	TEST HARDWARE	DARK GREY	
	ROM CHECKSUM	- RED	ROM U6
	RAM TEST	- GREEN	RAM, AGNUS, GARY
	CUSTOM REQ.	- BLUE	AGNUS, DENISE AND PAULA
	UNDEFINED FAILURE	- YELLOW	
6	TEST SOFTWARE	- LIGHT GREY	
7	SET UP DMA & INTERRUPT		
8	START DEFAULT TASK		

KEYBOARD POWER UP SELF TEST

ERROR-CODE	–	CAPLOCK LED
1 FLASH	–	ROM CHECKSUM FAILURE
2 FLASH	–	RAM FAILURE
3 FLASH	–	CLOCK FAILURE

SYSTEM DIAGNOSTIC

TEST	CAUSE
KEYBOARD MATRIX TEST	KEYBOARD, KB CPU 8520 U7, PAULA
BIT PLANE IMAGES	8371 AGNUS, DENISE, RAM
MOUSE	MOUSE, U15 74LS157, DENSISE, U7 8520, PAULA
ANIMATION	AGNUS
RTC	GARY, 6242, XTAL 32768, BATTERY
AUDIO	PAULA, LF347/TL084
LED ON/OFF	U7 8520, U38, Q301 2N3906
SPRITES	AGNUS, DENISE
CHIP RAM	RAM , AGNUS, GARY LS273
FAST RAM	F244
DISK	DISK DRIVE, CABLE PAULA,8520 GARY

PRODUCT: A588

No :8988-883
Page : 1 of 2

Subject: To convert A1000 diagnostic board for A500

1 Remove all LEDs on U23 and replace it with an IC socket.
2 Remove resister pack on U22 and replace it with an IC socket
3 Connect pin 9 of U23 to pin 12 of J8
4 Cut trace under pin 12 of J8
5 Connect pin 10 of U23 to pin 11 of J8
6 Cut trace under pin 11 of J8
7 Connect pin 11 of U23 to pin 12 of U12
8 Connect pin 12 of U23 to +5V
9 Connect pin 14 of U23 to pin 3 of RN5
10 connect 1K resistor from pin 15 of U23 to GND
11 connect 1K resistor from pin 16 of U23 to GND
12 connect pin 15 of U23 to pin 18 of U26
13 connect pin 16 of U23 to pin 4 of U26
14 cut trace connecting pin 16 of J8 to GND
15 connect pin 16 of J8 to pin 13 of U26
16 cut trace connecting pin 23 of J8
17 cut trace connecting to pin 25 of J8
18 connect pin 9 of U22 to top of SW1 (the one not grounded)
19 connect pin 17 of J6 to pin 5 of U25
20 connect pin 13 of U12 to pin 19 of U25
21 connect pin 2 of RN4 to +5V
22 cut trace connecting pin 3 of U8 to pin 25 of J8
23 remove resistor R15
24 remove jumper under resistor R15

Test code LED connection

U22 pin	
3	D7
5	D6
2	D5
6	D4
1	D3
7	D2
4	D1
8	D0

Keyboard connector

U23		cd		
KB pin	9	pin	1	data
	10		2	clock
	11		3	reset
	12		4	+5V
	13		5	
	14		6	key
	15		7	GND
	16		8	status

connector function

J6	SERIAL
J7	EXTERNAL DRIVE
J8	PRINTER
J11	J/S 2
J12	J/S 1

connector pin assignment

26 14
13 1
(solder side)

A500 ROM BASED DIAGNOSTIC

Test 1.	Check ability to read last ROM location This is a general test of processor and 86 pin connector
Test 2.	Set serial port as input, test busy pout
Test 3.	DRDY and ACK test
Test 4.	Check the CBM Serial Bus
Test 5.	Check RTS-CTS bit set loop
Test 6.	Check RTS-CTS bit clear loop
Test 7.	Check DTR-DSR bit set loop
Test 8.	Check DTR-DSR bit clear loop
Test 9.	Roll a zero through the parallel port
Test a.	Roll a one through the parallel port
Test b.	Write/Read a "?" character via the serial connection
Test c.	Write/Read an "E" character via the serial connection
Test d.	Write/Read a "J" character via the serial connection
Test e.	Write/Read a "string" char. via the serial connection
Test f.	Keyboad communication test
Test 10	"SEL" line set as input, reset, except "CD" to be set
Test 11	"SEL" line set as input, toggel and check "CD"
Test 20	Check parallel port reset line
Test 21	Check disk port reset line
Test 22	Check serial port reset line
Test 23	Check parallel port reset line can be set

Test 24 Check disk port reset line can be set

Test 25 Check serial port reset line can be set

Test 26 Check fire lines as output, check if set

Test 27 Check fire lines as output, check if cleared

Test 28 Check fire 1 lines as output

Test 29 Check fire 0 lines as input

Test 2a Check fire 1 lines as input

Test 2b Check fire 0 lines as input

Test 2c Check fire 1 lines as input

Test 2d Check fire 0 lines as input

Test 30 Verify keyboard +5 volts is o.k.

Test 31 Verify serial port +5 volts is o.k.

Test 32 Verify j/stick [1] +5 volts is o.k.

Test 33 Verify j/stick [0] +5 volts is o.k.

Test 34 Verify d/drive +5 volts is o.k.

Test 35 Check keyboard ground keyboard connector

Test 36 Check internal Disk ground Internal disk connector

Test 37 Check external disk ground external disk connector

Test 38 Check serial port ground number 2 serial connector

Test 39 Check serial port ground number 1 serial connector

Test 3a Check joystick [1] ground

Test 3b Check joystick [0] ground

Test 47 Table drive joystick position checking

Test 50 Set all pot lines to output (pull down) verify all low

Test 51 Toggle pot [x] port [1], verify line goes hi

Test 52 Toggle pot [y] port [1], verify line goes hi

Test 53 Toggle pot [x] port [0], verify line goes hi

Test 54 Toggle pot [y] port [0], verify line goes hi

Test 55 Set all pot lines to output (pull up) verify all high

Test 56 Toggle pot [x] port [1], verify line goes lo

Test 57 Toggle pot [y] port [1], verify line goes lo

Test 58 Toggle pot [x] port [0], verify line goes lo

Test 59 Toggle pot [y] port [0], verify line goes lo

Test 5a Set up to begin testing the pots as input

Test 5b Pot input load testing on all

Test 5c Pot input load testing on pot x port 1

Test 5d Port input load testing on pot y port 1

Test 5e Port input load testing on pot x port 0

Test 5f Port input load testing on pot y port 0

Test 60 Test external disk control lines

Test 6a Test internal disk control lines and ground line

Test 6b Test light pen function

Test 72 Test disk RESPONSE line

Test 76 Test disk RESPONSE "INDEX" line

Test 77 Try to force a reset test with a "NARROW" pulse

Test 78 Memory bit checking

Test 79 Complimentary bit checking

Test 7a Sliding ZEROS pattern

Test 7b Sliding ONES pattern

Test 7c Address as DATA test

Test 7d Inverted address as DATA test

Test 7e Bytefill test

Test 80 ROM checksum checking

Test 81/87 RAM/ROM memory check

Test 83 Test ROM/RAM strobe

Test 84 Test ROM/RAM address lines

Test 85 Test ROM/RAM pattern

Test 88 WRITE protect on ROM/RAM

Test 89 Check the four Audio channels, and Audio DMA

Test 90 Custom chip register testing, clear ADKCON

Test 91 Check ADKCON set and clear bit loop

Test 92 Custom chip register testing, clear CLXDAT

Test 93 Check DMACOON [R] resistor

Test 94 Check INTREQ resistor

Test 95 Check INTENA resistor

Test 96 Test joystick resistor pattern #1

Test 97 Test joystick resistor pattern #2

Test 98 Test joystick resistor pattern #3

Test 99 Test joystick resistor pattern #4

Test fO Check Ram Bus bits 8,9,10,11

Test f1 Check Ram Bus bits 12,13,14,15

Test f2 Check Ram Bus bits O,1,2,3

Test f3 Check Ram Bus bits 4,5,6,7

Test f4 Check Ram Bus bits 8,9,10,11

Test f5 Check Ram Bus bits 12,13,14,15

Test f6 Check Ram Bus bits O,1,2,3

Test f7 Check Ram Bus bits 4,5,6,7

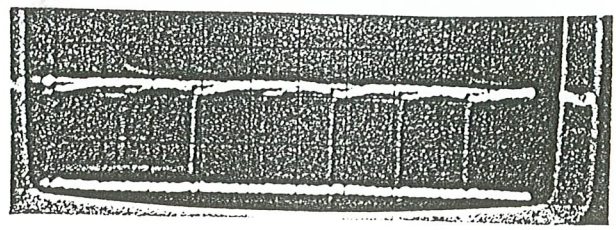
STEP 5

SIGNAL A1-A23

TEST POINT 68000 PIN 29

OSC SETTING .2M S/DIV

POSSIBLE CAUSE
GARY, 68000, ROM, 8520
AGNUS.



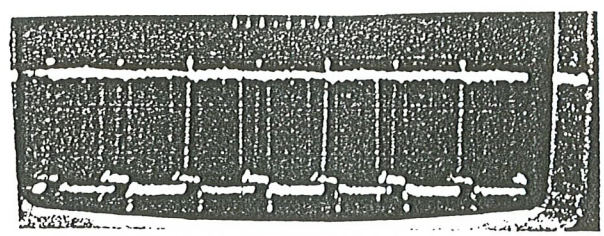
STEP 6

SIGNAL DTACK

TEST POINT 68000 PIN 10

OSC SETTING .2M S/DIV

POSSIBLE CAUSE
GARY



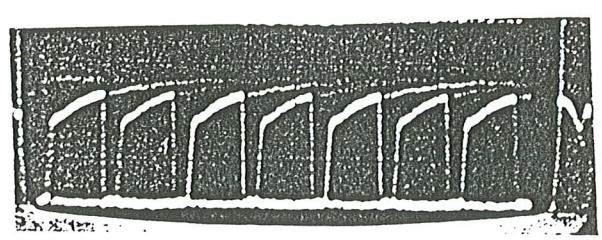
STEP 7

SIGNAL AS, UDS, LDS

TEST POINT 68000 PIN 6, 7, 8

OSC SETTING .2M S/DIV

POSSIBLE CAUSE
68000, ROM, GARY, AGNUS



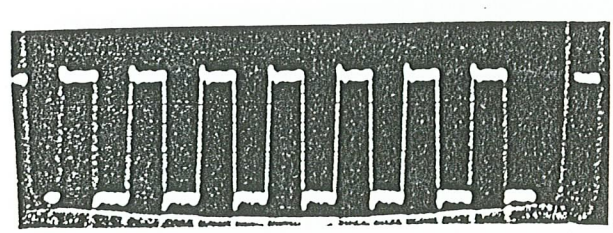
STEP 8

SIGNAL LATCH

TEST POINT GARY PIN 25

OSC SETTING .2M S/DIV

POSSIBLE CAUSE
GARY



WAVEFORM COMPARISON

STEP 1

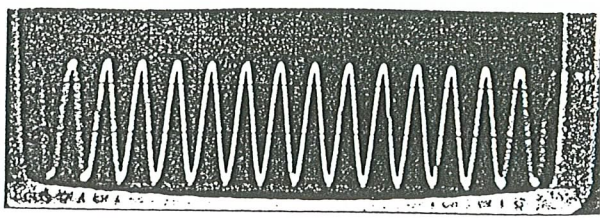
SIGNAL 28 MHz

TEST POINT XTAL X1 PIN O/P

OSC SETTING .05 μ S/DIV

POSSIBLE CAUSE

XTAL



STEP 2

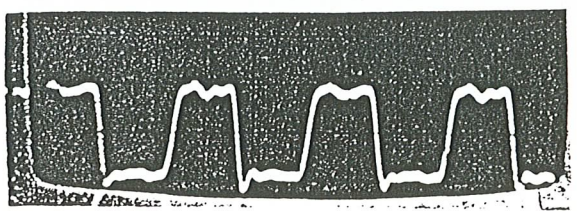
SIGNAL CLK

TEST POINT 68000 PIN 15

OSC SETTING .05 μ S/DIV

POSSIBLE CAUSE

AGNUS



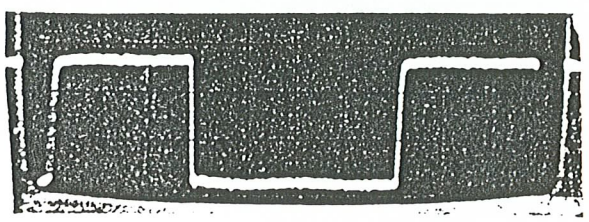
STEP 3

SIGNAL E

TEST POINT 68000 PIN 20

OSC SETTING .2 μ S/DIV

POSSIBLE CAUSE



STEP 4

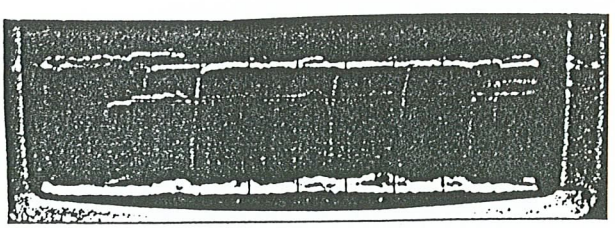
SIGNAL D0 - D15

TEST POINT 68000 PIN 5

OSC SETTING .2 μ S/DIV

POSSIBLE CAUSE

68000, ROM, VIO, VI2, 8520



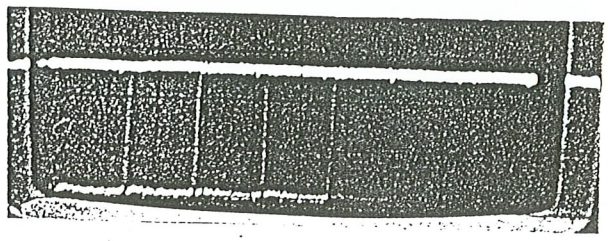
STEP 9

SIGNAL DEB

TEST POINT GARY PIN 4

OSC SETTING .2 M S/DIV

POSSIBLE CAUSE
GARY



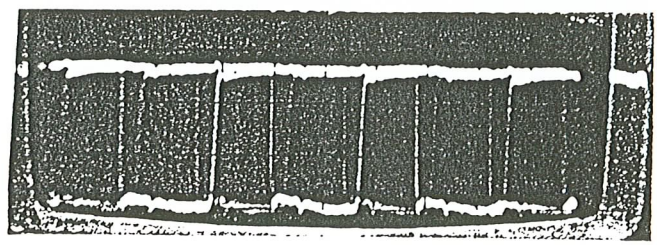
STEP 10

SIGNAL ROMEN

TEST POINT GARY PIN 21

OSC SETTING .2 M S/DIV

POSSIBLE CAUSE
GARY



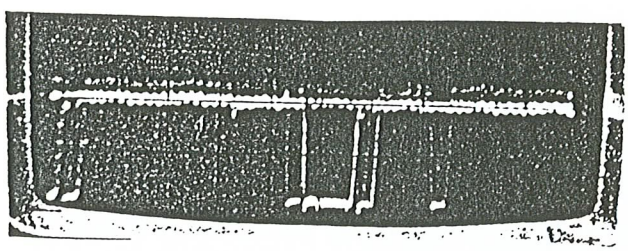
STEP 11

SIGNAL RGA1-RGA8

TEST POINT AGNUS PIN ____

OSC SETTING .2M S/DIV

POSSIBLE CAUSE
AGNUS



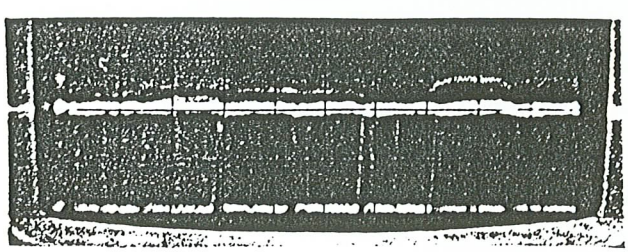
STEP 12

SIGNAL DRA0-DRA8

TEST POINT AGNUS PIN ____

OSC SETTING .2 M S/DIV

POSSIBLE CAUSE
AGNUS



STEP 13

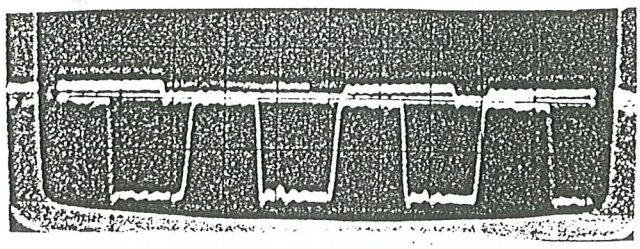
SIGNAL CASL, CASH

TEST POINT AGNUS PIN 54, 55

OSC SETTING .1 S/DIV

POSSIBLE CAUSE

AGNUS



STEP 14

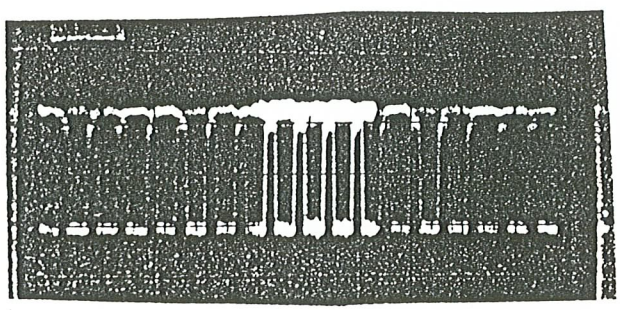
SIGNAL RAS0

TEST POINT AGNUS PIN 57

OSC SETTING 0.5 M S/DIV

POSSIBLE CAUSE

AGNUS



STEP 15

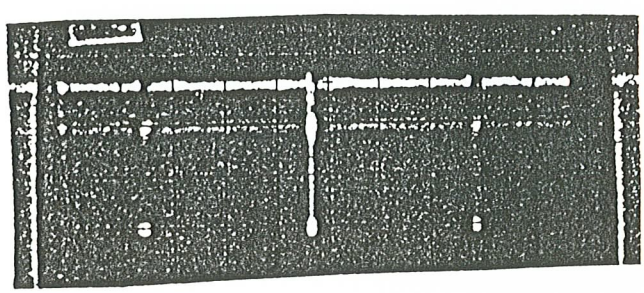
SIGNAL RAS1

TEST POINT AGNUS PIN 56

OSC SETTING 20M S/DIV

POSSIBLE CAUSE

AGNUS



STEP 16

SIGNAL DRD0-DRD15

TEST POINT 8364 PIN 10

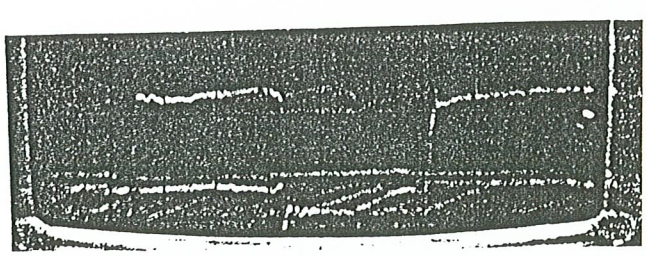
OSC SETTING .2 M S/DIV

POSSIBLE CAUSE

RAM, AGNUS, DENISE, PAULA,

U12, U10, U13, U11

F244 LS373



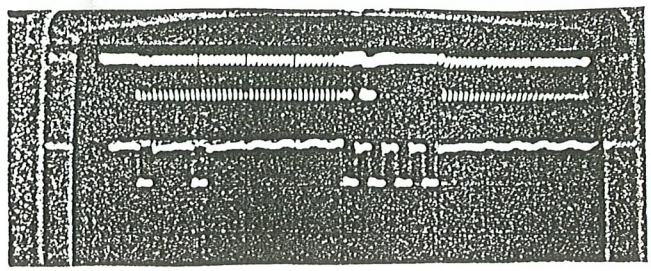
STEP 17

SIGNAL PBR

TEST POINT AGNUS PIN 20

OSC SETTING 10×5 1MS S/DIV

POSSIBLE CAUSE
AGNUS



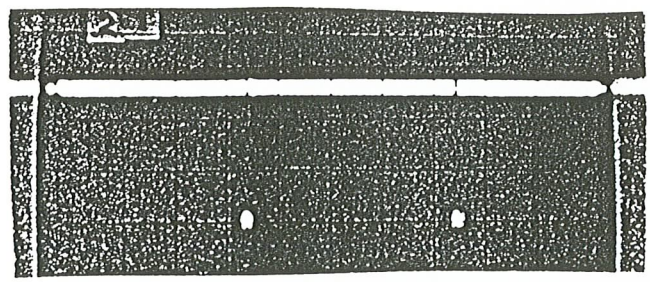
STEP 19

SIGNAL IPL P.1

TEST POINT 8364 PIN 13, 14

OSC SETTING 5μ S/DIV

POSSIBLE CAUSE
PAULA, 8520, AGNUS



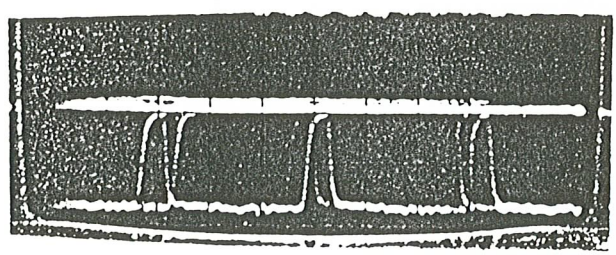
STEP 20

SIGNAL DRAM ADDRESS

TEST POINT RAM PIN 1

OSC SETTING .1μ S/DIV

POSSIBLE CAUSE
DRAM, U34



STEP _____

SIGNAL _____

TEST POINT _____ PIN _____

OSC SETTING _____ S/DIV

POSSIBLE CAUSE

DRAM REFRESH WAVEFORM - CPU REMOVED

STEP _____

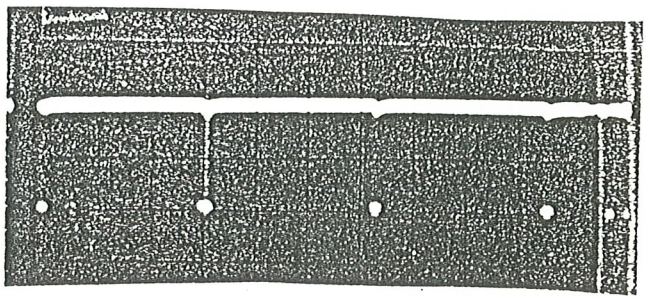
SIGNAL RAS

TEST POINT DRAM PIN 4

OSC SETTING .05M S/DIV

POSSIBLE CAUSE

AGNUS



STEP _____

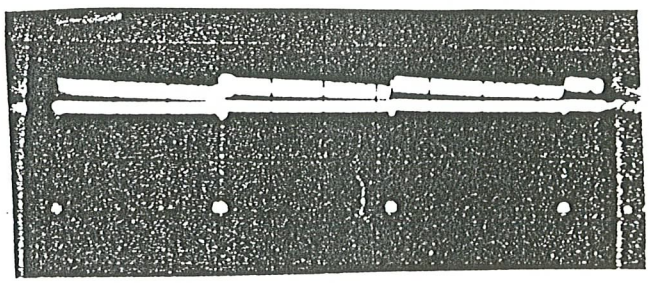
SIGNAL ADDRESS

TEST POINT DRAM PIN 5

OSC SETTING .05M S/DIV

POSSIBLE CAUSE

AGNUS, DRAM, U34



STEP _____

SIGNAL _____

TEST POINT _____ PIN _____

OSC SETTING _____ S/DIV

POSSIBLE CAUSE

STEP _____

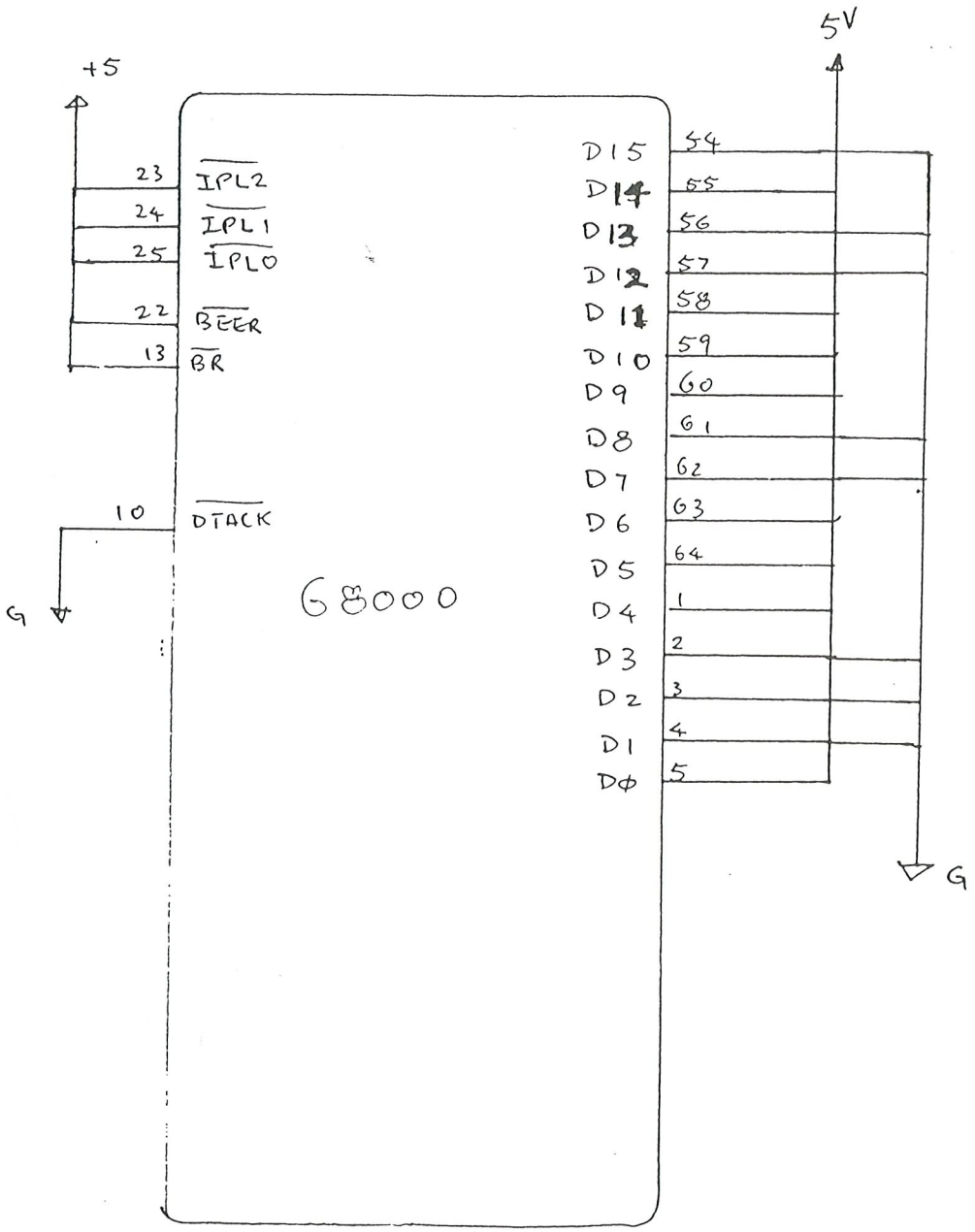
SIGNAL _____

TEST POINT _____ PIN _____

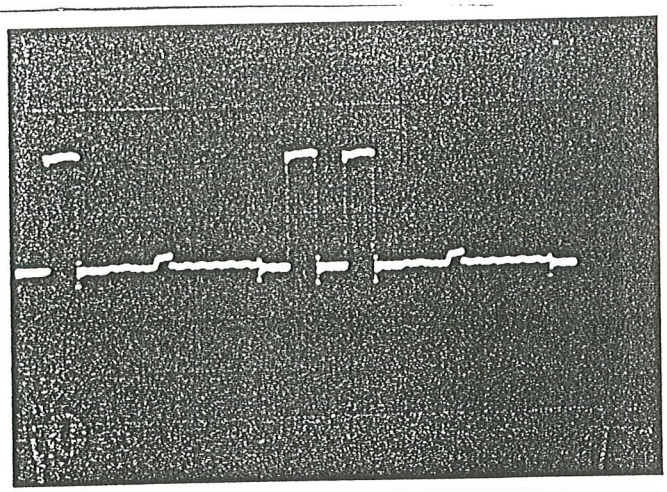
OSC SETTING _____ S/DIV

POSSIBLE CAUSE

NO OPT 68000



NOP
IS
0 1 00 111 00 111 0001 0

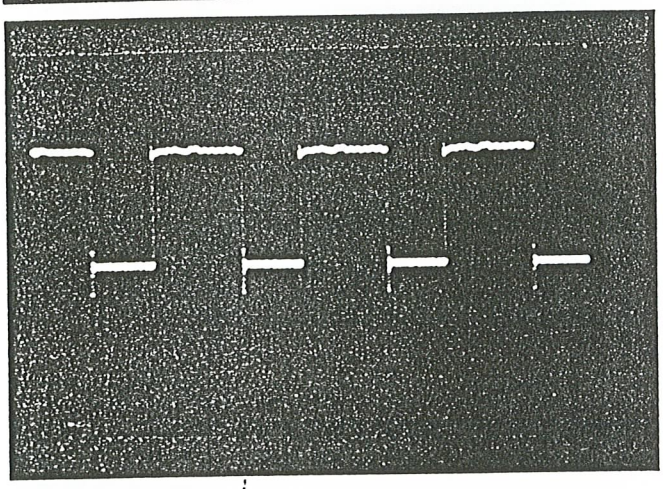


NO - OFF

A1, A2
1μs

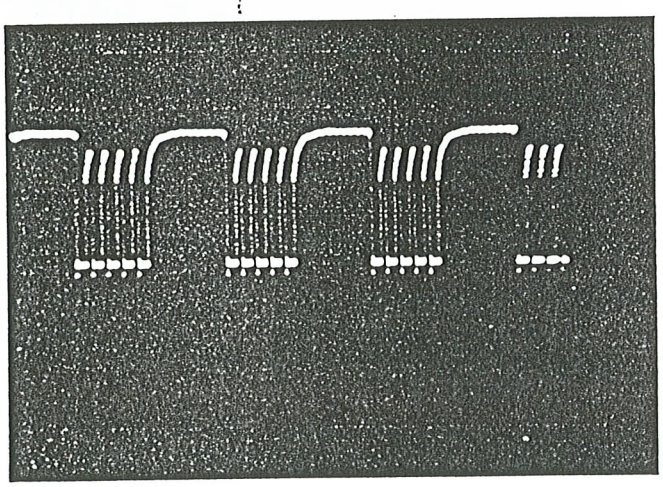
'0' A3, A7, A15
A17, A18, A23

'1'



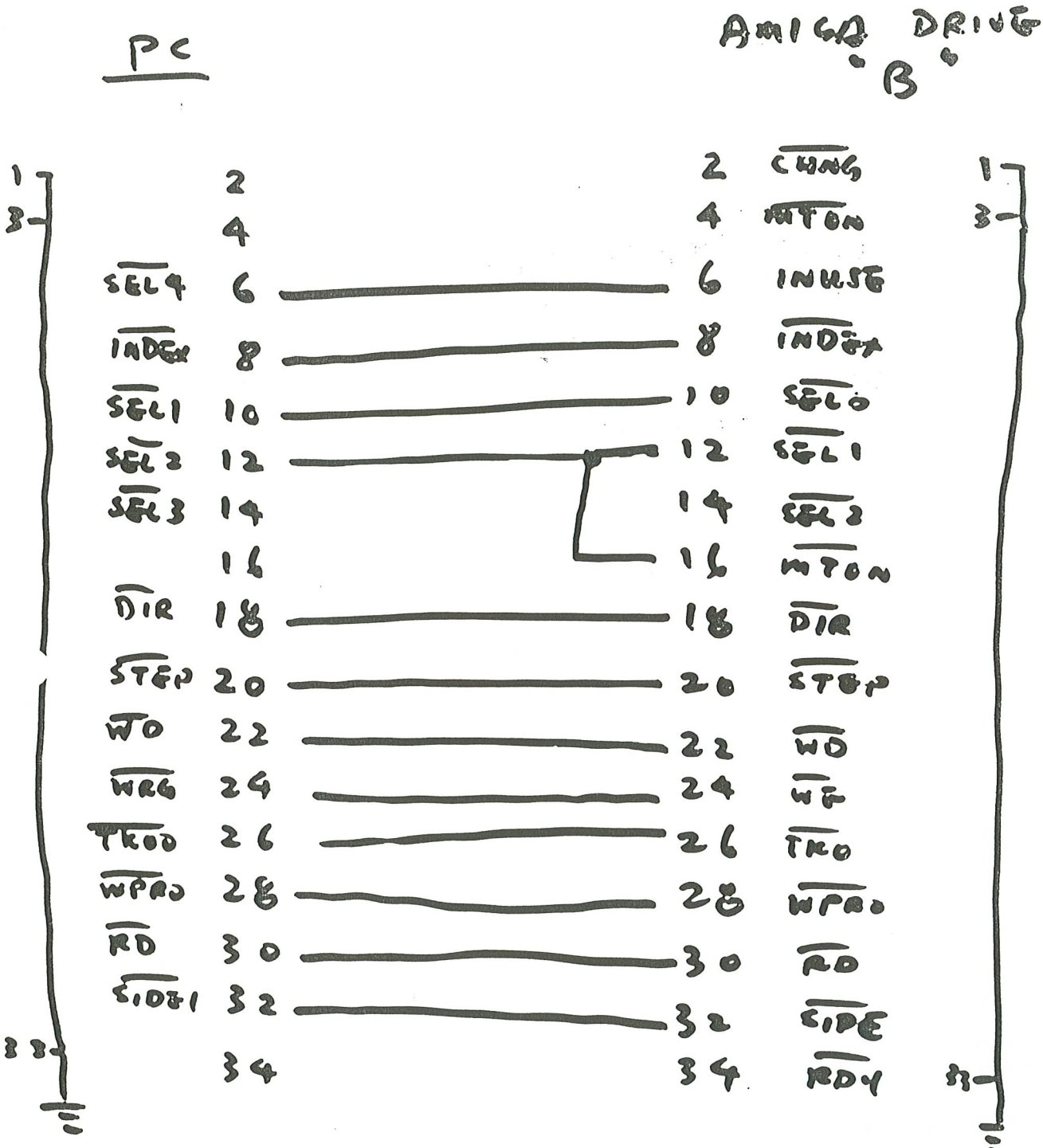
2μs
A4, A5, A6, A9,
A14, A16, A20, A21
A22

A12, A13 1.5V



A 2μs
A5, UDS, LDS

DISK DRIVE ALIGNMENT ADAPTOR CABLE
(AMIGA DRIVE TO PC)



DRIVE MOTOR SPEED ADJUSTMENT

If the reading from the Speed Test is not within the allowed limits of 295-305, the motor speed must be adjusted. Although the procedure for this adjustment is the same for all drives, the location of the Motor Speed Control Pot will vary. The Internal Drive Mechanism can be identified once the Amiga Top Shield and RF Shield have been removed. The External Drive Mechanism can be identified once the top has been removed from the External Drive.

DRIVE VENDOR IDENTIFICATION

1. NEWTRONICS DRIVE ASSEMBLY - Label on back of the Drive Mechanism ...

```
*****************************
* D357                      *
* MITSUMI ELEC. CO., LTD    *
* MADE IN JAPAN             *
*****************************
```

2. PANASONIC DRIVE ASSEMBLY - Label on the top of the drive Mounting Bracket..

```
*******************************
* MODEL  JU-363-Ø3            *
* MATSUSHITA COMMUNICATION    *
* MADE IN JAPAN               *
*******************************
```

3. NEC DRIVE ASSEMBLY - Label on the back of the Drive Mechanism..

```
*******************************
* FD1Ø35                      *
* NEC CORPORATION             *
* MADE IN JAPAN               *
*******************************
```

4. CHINON DRIVE ASSEMBLY - Label on the side of the drive Mechanism..

```
*******************************
* F-354E                      *
* CHINON IND,INC.             *
* MADE IN JAPAN               *
*******************************
```

The Motor Speed is adjusted by turning the Motor Speed Control POT until the displayed speed reading is equal to (3ØØ). the location of the Motor Speed Control POTS are listed below.

(A) NEWTRONICS - Top Right Hand Side of the Drive Mechanism behind the Plastic Plate. Accessed from the top of the Drive Assembly.

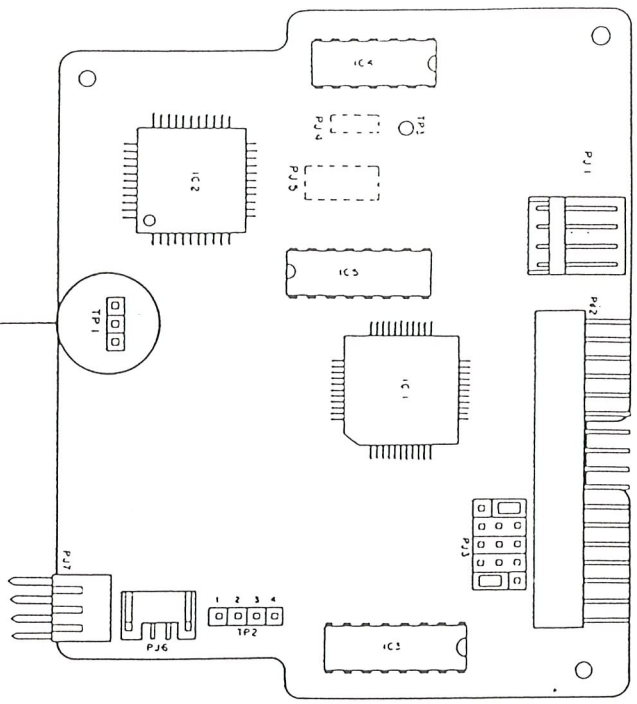
(B) PANASONIC - Designated as (VR1) on the Drive PCB. Accessed from the bottom of the Drive Assembly.

(C) NEC - Designated as (VR1) on the Drive PCB. Accessed from the bottom of the Drive Assembly.

(D) CHINON - Designated as (VR1) on the Drive PCB. Accessed from the bottom of the Drive Assembly.

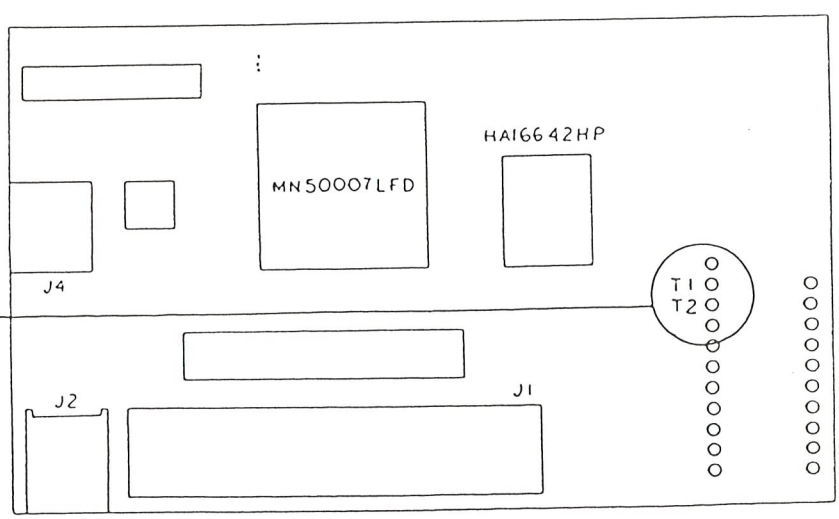
CHINON
(F - 354E)

ALIGNMENT TEST POINTS
USE - TP1, 1ST AND 3RD PINS



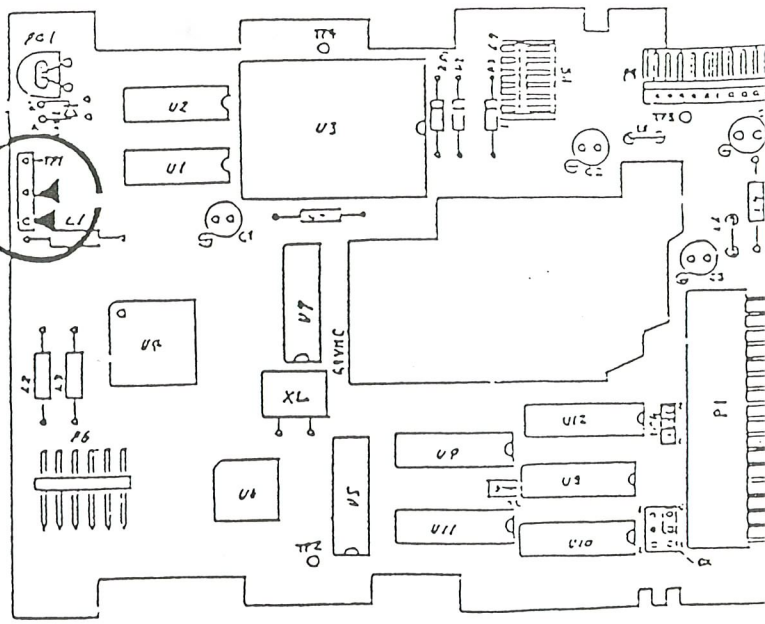
PANASONIC
(MATSUSHITA JU363 - 03)

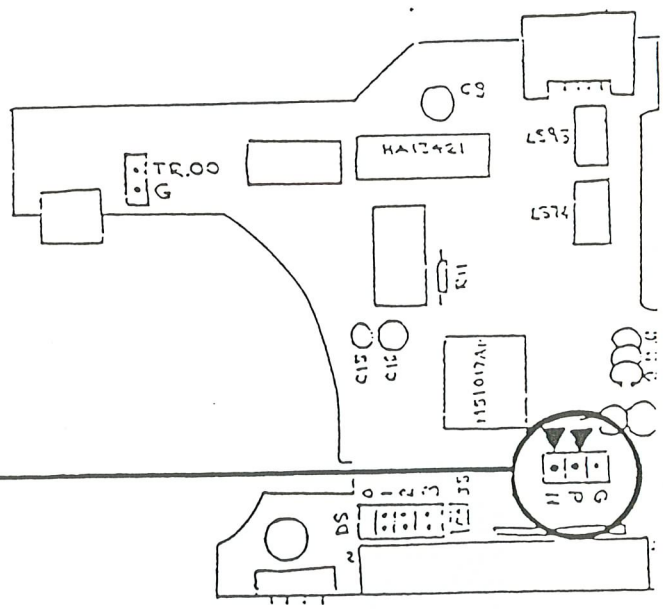
ALIGNMENT TEST POINTS
USE - T 1 AND T 2



NEC
(FD1035-008)

ALIGNMENT TEST POINTS
USE - TP1, 2ND AND 3RD LEADS





NEWTRONICS
(MITSUMI D357)

ALIGNMENT TEST POINTS
USE - N AND P